CH641 Datasheet

V1.7

http://wch-ic.com

Overview

CH641 series is a dedicated microcontroller for PD wireless charging designed based on QingKe RISC-V2A core. This series has a wide voltage, 1-wire serial debug interface, low-power consumption, peripheral streamlining, etc. CH641 built-in PD PHY, BC interface, differential input current sampling and AC small signal amplification decoder, support USB PD and Type C fast charging function, BC1.2 and DCP and a variety of other high-voltage charging protocols, provides DMA controller, 10-bit ADC, multi-group timer, USART, I2C and other rich peripheral resources, providing over-voltage protection and over-temperature protection.

Feature

- **Core**
- QingKe 32-bit RISC-V core, RV32EC instruction set
- Fast programmable interrupt controller + hardware interrupt stack
- Support 2-level interrupt nesting
- Support system main frequency 48MHz
- **Memory**
- 2KB volatile data storage area SRAM
- 16KB program memory area CodeFlash
- 1920B System BootLoader storage area
- 64B system non-volatile configuration information memory area
- 64B user-defined information storage area
- **Power management and low-power:**
- System power supply V_{HV} rated voltage: 5V~12V
- Internally generated V_{DD} voltage for I/O and simulation: 4.8V
- Low-power modes: Sleep, Stop, Standby
- **Clock & Reset**
- Built-in factory-tuned 24MHz RC oscillator
- Built-in low frequency RC oscillator
- Power on reset, programmable voltage detector
- **7-channel general-purpose DMA controller**
- 7 channels, support ring buffer management
- Support TIM1/ADC/USART/I2C
- **1 set of 10-bit ADC**
- Analog input range: GND ~ 3.3V
- 15-channel external signal channel+ 1-channel internal signal channel
- Support external delayed triggering
- **Multiple timers**
- 1×16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
- 1×16-bit streamlined general-purpose timers
- 1 watchdog timers (window watchdog)
- SysTick: 32-bit counter
- **1 set of USART with multi-pin mapping**
- **1×I2C slave interface**
- **USB PD and Type C controller and PHY**
- Support DRP, Sink, and Source applications
- 3 CC pins, some CC pins with built-in Rd
- **1×BC interface**
- Support BC1.2 and multiple HV DCP charging protocols
- Built-in 6-bit DAC, support a variety of voltage output and pull-up
- **Differential input current sampling ISP/ISN**
- **AC small signal amplifier and decoder QII**
- **GPIO port**
- 2 sets of GPIO port, 25 I/O ports
- External interrupt
- 4 high voltage drive pins, 5 low voltage strong drive pins
- **Overvoltage protection (OVP) and overtemperature protection (OTP)**
- **Security features: 64-bit Chip unique ID**
- **Debug mode: 1-wire serial debug interface**

(SDI)

- **Package: QFN**

Model	FLASH	SRAM	GPIO	Advanced-control timer	General-purpose timer	Serial port	I2C	System clock source	ADC	High voltage drive I/O	BC interface DAC	USB PD Type-C	Differential current sampling ISP	Signal decoding QII	Package form
CH641F	16K	2K	25	1	1	1	1	2	15+1	4	√	3 CC	√	√	QFN28
CH641D	16K	2K	17	1	1	1	1	2	10+1	4	√	3 CC	√	√	QFN20
CH641X	16K	2K	17	1	1	1	1	2	12+1	2	√	3 CC	√	√	QFN20
CH641P	16K	2K	13	1	1	1	-	2	10+1	2	√	3 CC	√	√	QFN16

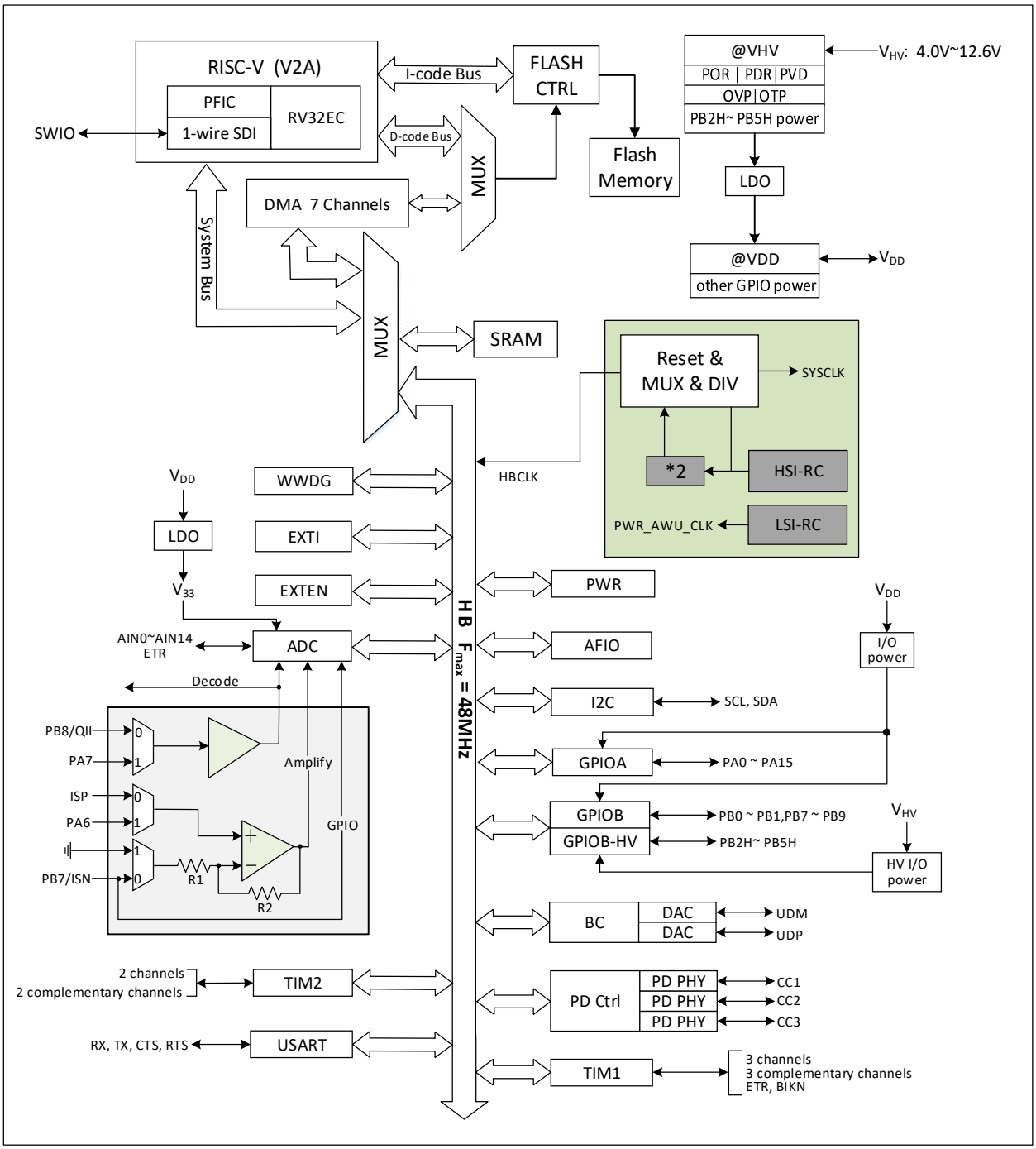
Note: The CH641X and CH641P provide only 2 high-voltage I/Os for wireless charging applications, but with more drive capability.

Chapter 1 Specification Information

1.1 System Structure

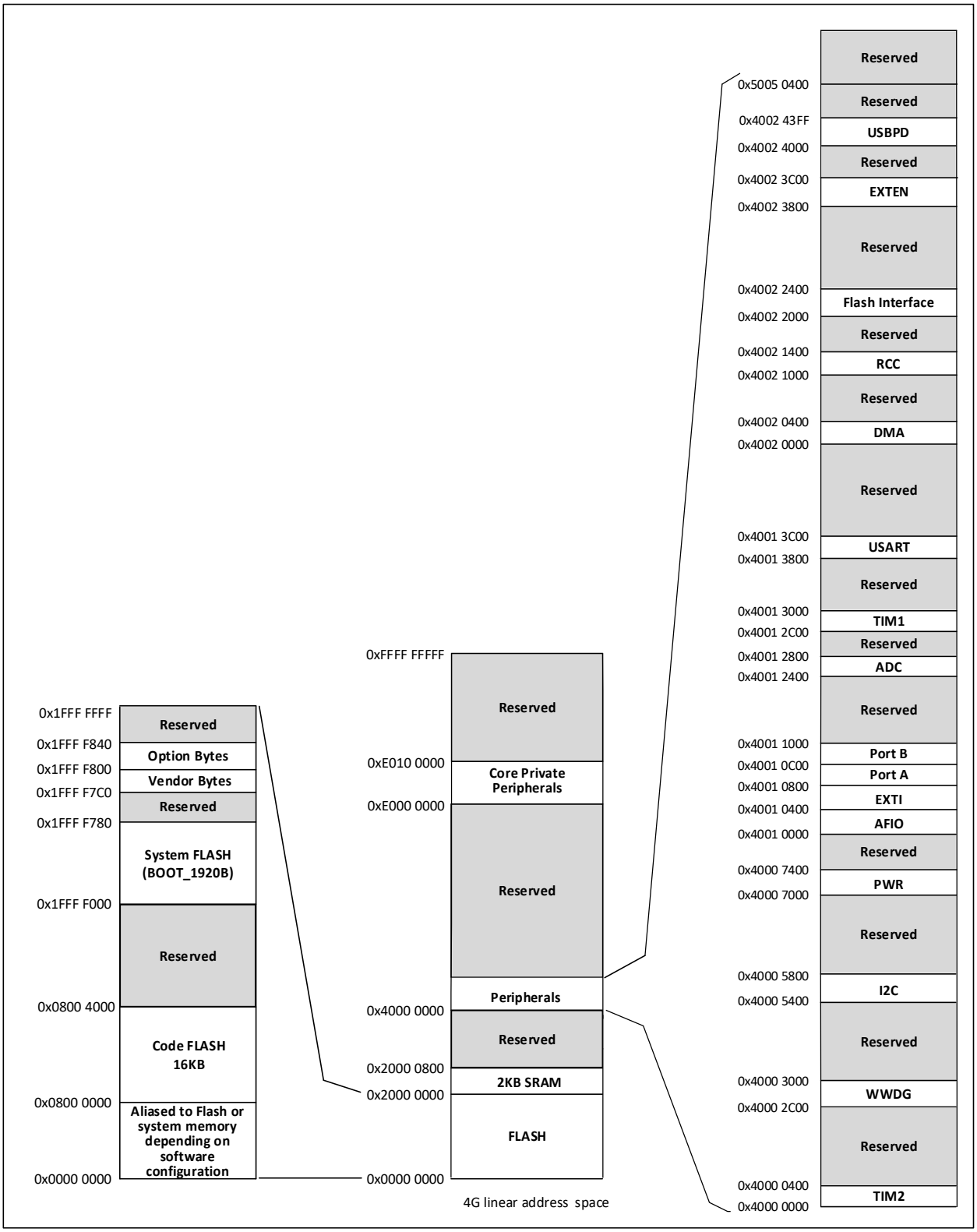
The microcontroller is based on the RISC-V instruction set QingKe V2A design, its architecture will be the core, arbitration unit, DMA module, SRAM storage and other parts of the interaction through multiple buses. The design integrates a general-purpose DMA controller to reduce the burden on the CPU, improve access efficiency, while both data protection mechanisms, automatic clock switching protection and other measures to increase system stability. The following diagram shows the overall architecture of the CH641.

Figure 1-1 MCU system block diagram



1.2 Memory Map

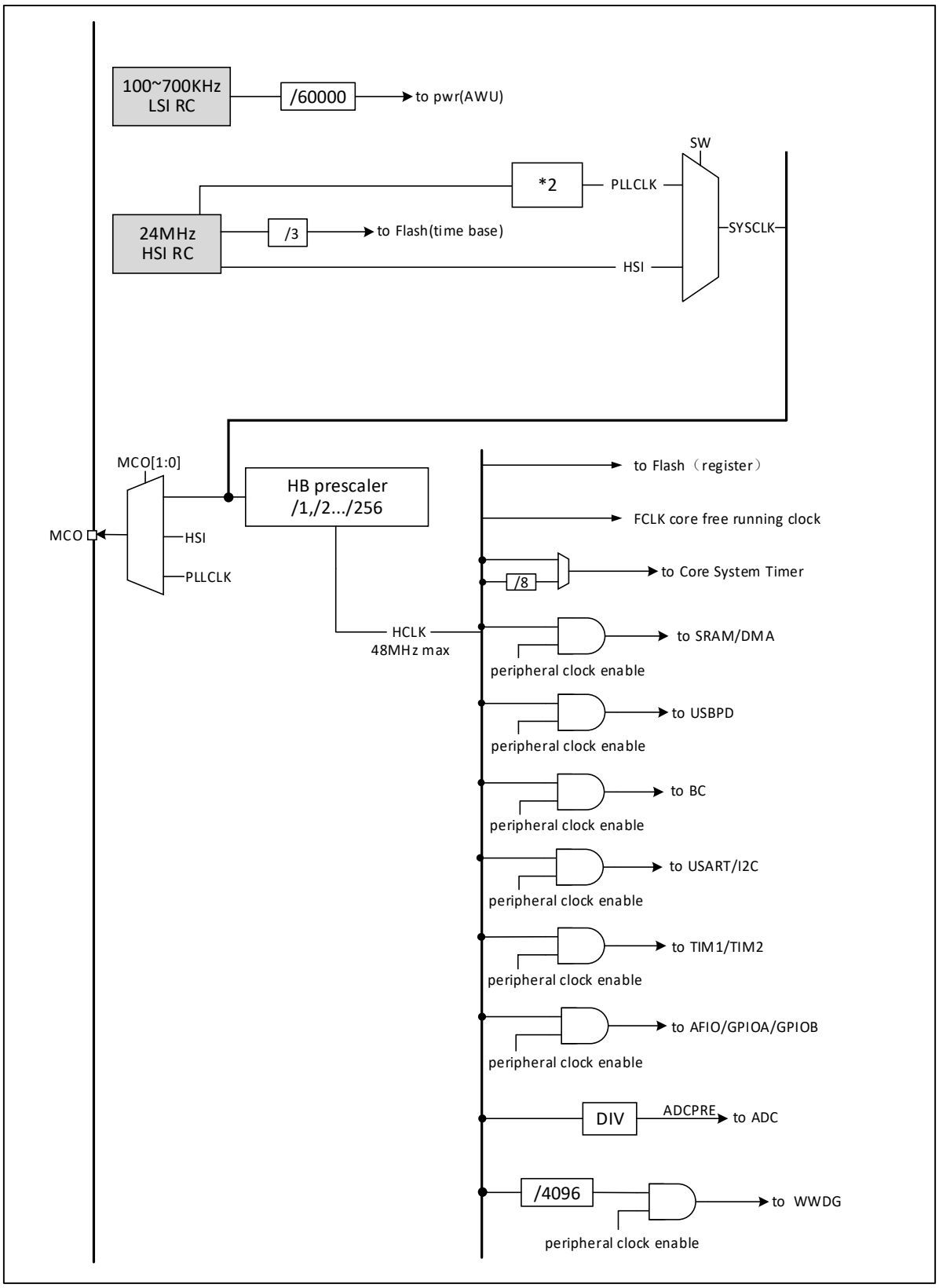
Figure 1-2 Memory address map



1.3 Clock Tree

2 sets of clock sources are introduced into the system: an internal high-frequency RC oscillator (HSI) and an internal low-frequency RC oscillator (LSI). Among them, the low-frequency clock source provides a clock reference for the automatic wake-up unit, and the high-frequency clock source is directly or indirectly output as the system bus clock (SYSCLK) through a 2x multiplier, and the system clock is then provided by the pre-scaler for the HB domain peripheral control clock and sampling or interface output clock.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V2A Processor

The RISC-V2A supports the EC subset of the RISC-V instruction set. The processor is internally managed in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), extended instruction support, and so on. The bus is connected to external unit modules to enable interaction between external function modules and the core.

QingKe processor with its minimalist instruction set, a variety of operating modes, modular customization and expansion features can be flexibly applied to different scenarios MCU design, such as small area low-power embedded scenarios.

- Support machine and user privileged modes
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- 1-wire serial debug interface (SDI)
- Custom extension instructions

1.4.2 On-chip Memory

Built-in 2K-byte SRAM area, which is used to store data, which is lost after power loss.

Built-in 16K-byte program flash memory area (Code FLASH), that is, the user area, is used for users' applications and constant data storage.

Built-in 1920-byte system storage area (System FLASH), that is, BOOT area, is used for system boot program storage (factory-solidified bootloader). After setting the user configuration word START_ mode bit to 0 to turn off BOOT, it can also be used for user applications and constant data storage (you need to use ld segmented link files).

Built-in 64-byte system non-volatile configuration information storage area, used for manufacturer configuration word storage, solidified before leaving the factory, users can not be modified.

Built-in 64-byte user-defined information store for user option byte storage.

Support Boot and user code to jump to each other.

1.4.3 Power Supply Scheme

Solution 1 (V_{DD} powered by internal LDO regulator): External power supply to V_{HV}: 4.0~12.6V. V_{HV} supplies power to the LDO and outputs the corresponding voltage on the V_{DD} pin. When $5.0V \leq V_{HV} \leq 12.6V$, the V_{DD} pin outputs the rated 4.8V. When $4.0V \leqslant V_{HV} < 5.0V$, the voltage output on the VDD pin decreases accordingly.

Solution 2 (V_{DD} optionally powered directly from external source): External power supply directly to V_{DD} at 3.5~5.5V is permitted, requiring $V_{HV} \geq V_{DD}$. Specifically, when $3.5V \leq V_{DD} \leq 4.8V$, V_{HV} and V_{DD} must be shorted.

V_{HV} = 4.0~12.6V: Supply power to the internal voltage regulator and 4 HV high voltage I/O pins. For applications above 9V, it is recommended that the cumulative capacitance on the V_{HV} is not less than 10uF.

V_{DD}: Supplies power to most of the I/O pins and analog modules, usually requiring external high-frequency decoupling capacitors with 1uF or 2.2uF capacity.

V_{33}: The internal voltage regulator generates 3.3V, which provides a reference voltage for the ADC inside the chip.

1.4.4 Power Supply Monitor

The power-on reset (POR) / power-down reset (PDR) circuit is integrated inside the CH641, when the V_{HV} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without the need to use an external reset circuit.

In addition, the system has a programmable voltage detector (PVD), which needs to be turned on by software, which is used to compare the voltage of V_{HV} power supply with the set threshold V_{PVD}. When the corresponding edge interrupt of the PVD is turned on, an interrupt notification can be generated when the V_{HV} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for the values of $V_{POR/PDR}$ and V_{PVD}.

CH641 also has built-in abnormal protection modules such as OVP and OTP, which will forcibly reset the MCU when the V_{HV} voltage is too high or the chip temperature is too high.

1.4.5 System Voltage Regulator LDO

After reset, the regulator turns on automatically, and there are two operation modes according to the application mode.

- On mode: normal operation, providing stable core power supply
- Low-power mode: CPU stops and the system automatically enters Standby mode

1.4.6 Low-power Mode

The system supports two low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in operating state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: any interruption or wake-up event.

- Standby mode (STANDBY)

Set PDDS, SLEEPDEEP bit, execute WFI/WFE instruction to enter. In this mode, the high frequency clock (HSI/PLL) domain is turned off, the SRAM and register contents are maintained, and the state of the I/O pin is maintained, which can achieve the lowest power consumption. After waking up in this mode, the system can continue to run, with HSI as the default system clock source.

Exit conditions: any external interrupt / event (EXTI signal), external reset signal on RST, USBPD wake-up signal, PVD output, AWU automatic wake-up, in which the EXTI signal includes one of 25 external I/O ports.

1.4.7 Fast Programmable Interrupt Controller (PFIC)

The QingKe core MCU has a built-in Fast Programmable Interrupt Controller (PFIC), which supports up to 255 interrupt vectors and provides flexible interrupt management with minimum interrupt delay. CH641 manages 4 core private interrupts and 25 peripheral interrupt management, while other interrupt sources are retained. The registers of PFIC can be accessed in machine privilege mode.

- 2 individually maskable interrupts
- Support Hardware Prologue/Epilogue (HPE) without instruction overhead
- Provide 2 Vector Table Free (VTF) for faster access to interrupt service routine
- Vector table support address or instruction mode
- Support 2-level interrupt nesting
- Support interrupt tail linking

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt / event controller contains a total of 16 edge detectors for generating interrupt / event requests. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or double edge) and can be shielded separately; the suspend register maintains all interrupt request states. EXTI can detect clock cycles whose pulse width is less than that of the internal HB. All 25 general-purpose I/O ports can be connected to the same external interrupt source.

1.4.9 General DMA Controller

The system has a set of general DMA controllers, manages 7 channels, flexibly handles the high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral devices, and supports ring buffer mode. Each channel has special hardware DMA request logic, which supports one or more peripheral access requests to memory. Access priority, transmission length, source address and destination address of transmission can be configured.

DMA for the main peripherals include: advanced timer TIM1, ADC, USART, I2C.

Note: DMA and CPU access the system SRAM after arbitration by the arbitrator.

1.4.10 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the 3-division of the internal 24MHz clock is used as the default CPU clock, and then another PLL clock can be selected. For low power modes that turn off the clock, the system will also use an internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

1.4.11 Analog-to-digital Converter (ADC)

CH641 has a built-in 10-bit ADC, supports up to 15 external channels and 1 internal channel sampling, programmable channel sampling time, and can achieve single, continuous, scan or intermittent conversion. The analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages. External event trigger conversion is supported, and the trigger source includes the internal signal and external pin of the on-chip timer. Support the use of DMA operations. The external trigger delay function is supported. After enabling this function, when the external trigger edge is generated, the controller delays the trigger signal according to the configured delay time, and the delay time immediately triggers the ADC conversion.

1.4.12 Timer and Watchdog

The timer in the system includes an advanced-control timer, a general-purpose timer, a watchdog timer and a system time base timer.

- Advanced-control timer

The advanced-control timer is a 16-bit automatic load increment/decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer

The general-purpose timer is a 16-bit auto-load progressive counter with a programmable 16-bit prescaler and two independent channels and their corresponding complementary output channels. Each independent channel supports input capture, output comparison, PWM generation and mono-pulse mode output, as well as simple dead-time control, but does not support DMA.

- Watchdog timer

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- SysTick timer

The QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.13 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

CH641 provides a set of USART. Support full-duplex asynchronous communication and half-duplex single-line communication, also support LIN (Local Internet), compatible with IrDA SIR ENDEC transmission codec specification and modem (CTS/RTS hardware flow control) operation, but also allow multiprocessor communication. It adopts fractional baud rate generator system and supports continuous communication of DMA operation.

1.4.14 I2C Bus

1 I2C bus interface, works in slave mode, completes all I2C bus specific timing, protocol, arbitration, etc., supports standard and fast communication speed, but does not support host mode.

The I2C interface provides 7-bit or 10-bit addressing and supports double-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator / verifier.

1.4.15 USB PD and Type C Controller

Built-in 1 USB Power Delivery controller and 3 PD transceiver PHY. Three CC pins are provided, of which PB0/CC1R and PB9/CC3R pins have built-in controllable Rd pull-down resistors defined by the type-C specification. PB1/CC2 pins do not provide Rd by default and can support customization.

Support USB type-C master-slave detection, automatic BMC codec and CRC, hardware edge control, support USB PD2.0 and PD3.0 power transmission control, support fast charging, support UFP/PD power-receiving Sink and DFP/PD power supply Source applications, DRP applications and dynamic switching.

1.4.16 BC Interface

CH641 provides a set of BC interfaces with PA0/UDP and PA1/UDM pins, built-in 6-bit DAC and output buffers, supports a variety of voltage output and input comparison, supports multi-stage pull-up and pull-down resistors, and supports a variety of high-voltage charging protocols such as BC1.2 and DCP.

1.4.17 Differential Input Current Sampling (ISP)

CH641 supports current sampling of differential input, plus milliohm sampling resistor, which can realize

low-side current sampling and differential amplification. The positive side of the differential input supports two pin selections, the default ISP pin is the positive end of the differential input, the PA6 pin can be selected as the positive side of the differential input, and the PB7/ISN pin is the negative side of the differential input. The result of the differential amplification is sent to the ADC for sampling through the ADC_IN8 channel. Single-side input mode is supported without ISN, saving PB7 can be used for ADC or GPIO.

1.4.18 AC Small Signal Amplifier and Decoder (QII)

Built-in multistage magnification and filter, support digital filtering, mainly used for FSK/ASK decoding, can achieve high quality and low bit error rate in the transmission process. Signal input supports two pin selections, default is PB8/QII pin, PA7 pin can be selected as input. The decoded result is sent to the ADC for sampling through the ADC_IN9 channel.

1.4.19 General-purpose Input and Output (GPIO)

The system provides 2 sets of GPIO ports with a total of 25 GPIO pins. Most GPIO pins can be configured by software as push-pull output, input (with or without pull-up, partial pull-down), or reused peripheral function ports.

Most GPIO pins are shared with digital or analog multiplexing peripherals, providing a locking mechanism to freeze the IO configuration to avoid accidental writing to the I/O register.

When PB8 is used as GPIO, only input or open-drain output is supported, but push-pull output is not supported.

PB2H, PB3H, PB4H and PB5H provide high-voltage I/O pins supplied by V_{HV}, and the rest are low-voltage I/O pins powered by V_{DD}.

PA2, PA3, PA4, PA5 and PA9 all have strong current driving ability, which is about twice as strong as that of other common I/O pins.

PB3H and PB4H have built-in pull-up resistors that cannot be closed; PB2H and PB5H have no built-in pull-up resistors; ISP and PB8/QII have no built-in pull-up resistors; PA0 and PA1 have built-in default off and adjustable pull-up resistors, which are adjusted and controlled by two groups of PUE and DAC in EXTEN_CTLR1, and can provide pull-up current. Three CC pins are provided, of which the PB0/CC1R, PB1/CC2R and PB9/CC3R pins have built-in pull-up current defined by the type-C specification, which is controlled by the CC_PU in the R8_PORT_CC of the corresponding pin; other GPIO pins have built-in pull-up resistors that are off by default and can be turned on.

PA4 and PA5 have built-in pull-down resistors that can be turned on and off by default; PA0 and PA1 have built-in pull-down resistors that are turned on, adjustable and closed by default, which are adjusted and controlled by two groups of PDE and DAC in EXTEN_CTLR1, and can provide pull-down current. If CC1/CC2/CC3 has an R suffix, it indicates an internal controllable Rd pull-down resistor as defined by the Type-C specification, enabled by default. The PB0/CC1R and PB9/CC3R pins incorporate built-in controllable Rd pull-down resistors. When used as GPIO push-pull outputs, it is recommended to disable the pull-down. The PB1/CC2 pin does not provide Rd by default but supports customization, controlled by the CC_PD bit in R8_PORT_CC for the corresponding pin. All other GPIO pins do not incorporate built-in pull-down resistors.

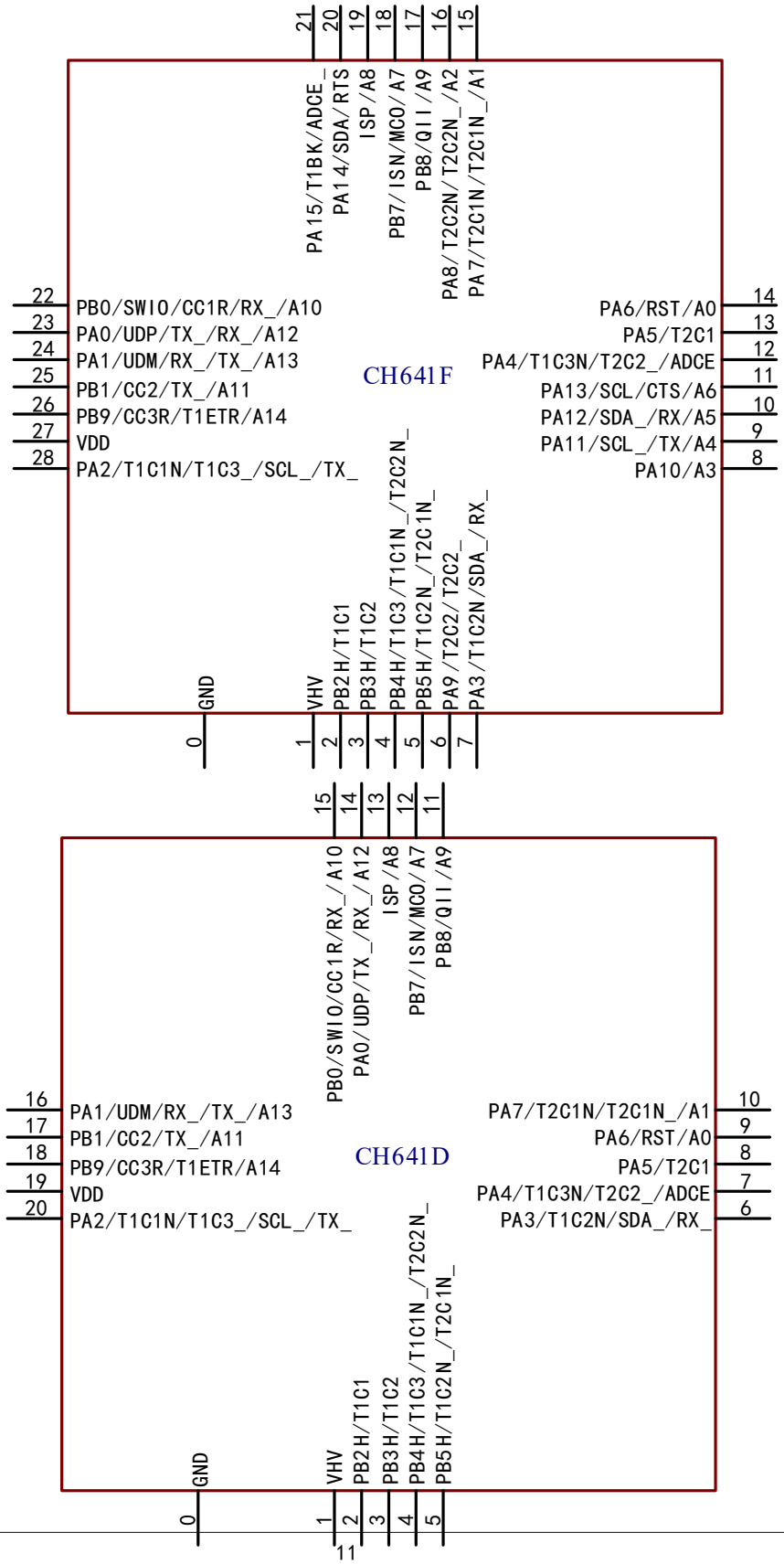
V_{HV} supplies power to the high-voltage I/O pin, which adapts to the external interface level by changing the VHV power supply to change the high value of the output level of the high-voltage I/O pin. The low-voltage I/O pin is powered by V_{DD} and adapts to the external interface level by changing the V_{DD} power supply to change the high value of the output level of the I/O pin. For specific pins, please refer to the description of the pins in Chapter 2.

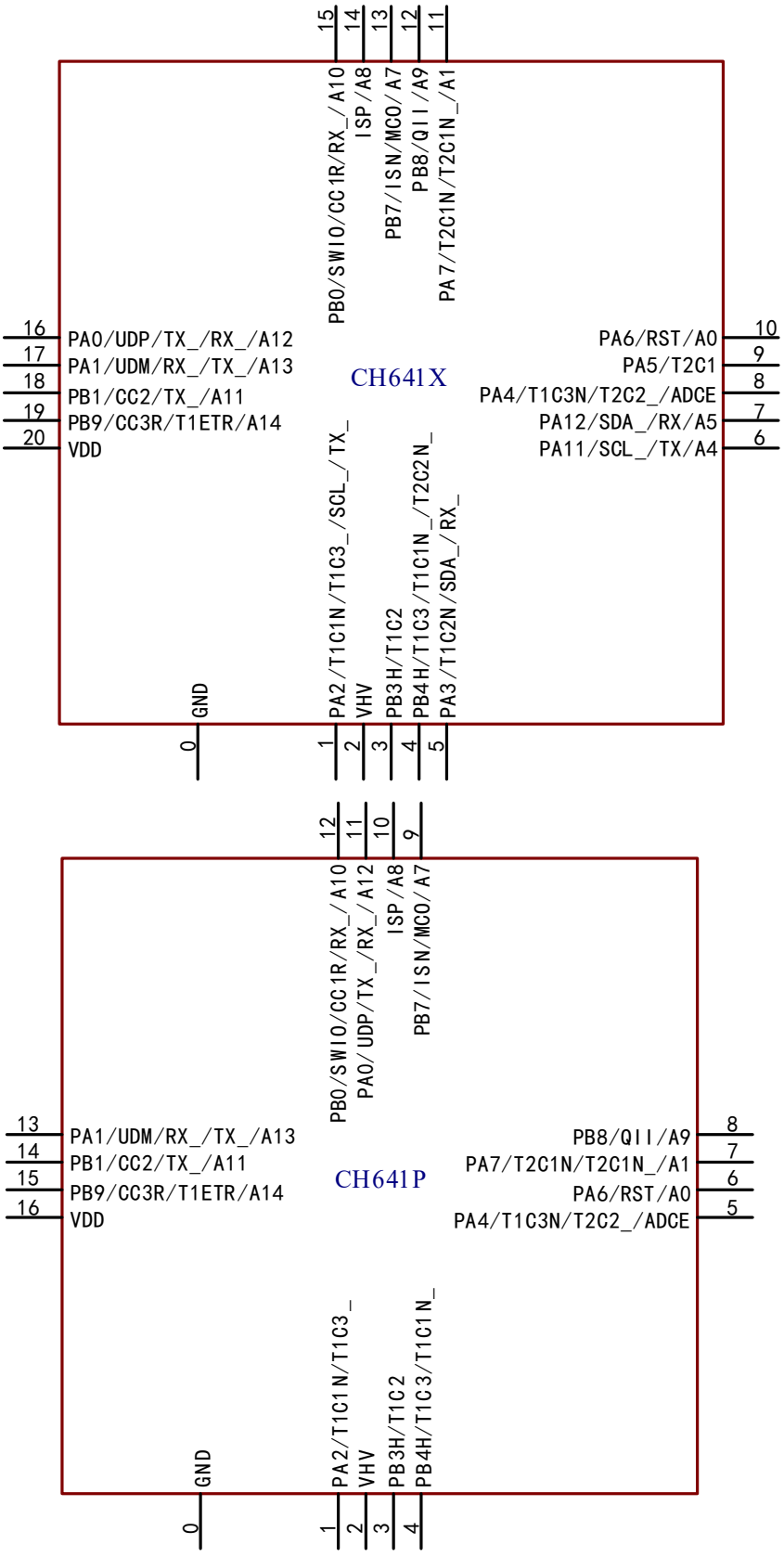
1.4.20 1-wire SDI Serial Debug Interface

The core comes with a serial 1-wire debug interface PB0/SWIO pin (Single Wire Input Output). The default debug interface pin function is on after the system is powered on or reset, and the program can be turned off after running.

Chapter 2 Pinouts and Pin Definition

2.1 Pinouts




CH641X
15 14 13 12 11
PB0/SWIO/CC1R/RX_/A10
ISP/A8
PB7/ISN/MCO/A7
PB8/QII/A9
PA7/T2C1N/T2C1N_/A1
16 PA0/UDP/TX_/RX_/A12
17 PA1/UDM/RX_/TX_/A13
18 PB1/CC2/TX_/A11
19 PB9/CC3R/T1ETR/A14
20 VDD
PA6/RST/A0 10
PA5/T2C1 9
PA4/T1C3N/T2C2_/ADCE 8
PA12/SDA_/RX/A5 7
PA11/SCL_/TX/A4 6
0 GND
1 PA2/T1C1N/T1C3_/SCL_/TX_
2 VHV
3 PB3H/T1C2
4 PB4H/T1C3/T1C1N_/T2C2N_
5 PA3/T1C2N/SDA_/RX_
CH641P
12 11 10 9
PB0/SWIO/CC1R/RX_/A10
PA0/UDP/TX_/RX_/A12
ISP/A8
PB7/ISN/MCO/A7
13 PA1/UDM/RX_/TX_/A13
14 PB1/CC2/TX_/A11
15 PB9/CC3R/T1ETR/A14
16 VDD
PB8/QII/A9 8
PA7/T2C1N/T2C1N_/A1 7
PA6/RST/A0 6
PA4/T1C3N/T2C2_/ADCE 5
0 GND
1 PA2/T1C1N/T1C3_
2 VHV
3 PB3H/T1C2
4 PB4H/T1C3/T1C1N_

Note: The reuse functions in the pin diagram are all abbreviations.

Example:

A: ADC_(A10: ADC_IN10)

T: TIME_(T1C3: TIM1_CH3, T1C1N:TIM1_CH1N, T1ETR: TIM1_ETR, T1BK: TIM1_BKIN)

TX (USART_TX)

RX (USART_RX)

CTS (USART_CTS)

RTS (USART_RTS)

SDA (I2C_SDA)

SCL (I2C_SCL)

ADCE (ADC_ETR)

Pin No.	Pin	Pin	I/O	Main	Default alternate	Remapping function

2.2 Pin Description

Table 2-1 Pin definition

Note: The pin function descriptions in the table below apply to all functionalities and do not pertain to specific chip models. Peripheral resources vary between different models. Before proceeding, please verify the availability of this feature by consulting the resource table for your specific chip model.

QFN16	QFN20(CH641X)	QFN20(CH641D)	QFN28						
0	0	0	0	GND	P	-	GND	-	-
2	2	1	1	V_{HV}	P	-	V_{HV}	-	-
-	-	2	2	PB2H	I/O	HV	PB2H	TIM1_CH1	-
3	3	3	3	PB3H	I/O	HV/PU	PB3H	TIM1_CH2	-
4	4	4	4	PB4H	I/O	HV/PU	PB4H	TIM1_CH3	TIM1_CH1N_1/TIM2_CH2N_2/TIM1_CH2N_3
-	-	5	5	PB5H	I/O	HV	PB5H	-	TIM1_CH2N_1/ TIM2_CH1N_2/TIM2_CH1N_3
-	-	-	6	PA9	I/O	LV	PA9	TIM2_CH2	TIM2_CH2_2
-	5	6	7	PA3	I/O	LV	PA3	TIM1_CH2N	I2C_SDA_1/USART_RX_4
-		-	8	PA10	I/O/A	-	PA10	ADC_IN3	-
-	6	-	9	PA11	I/O/A	-	PA11	ADC_IN4/USART_TX	I2C_SCL_2
-	7	-	10	PA12	I/O/A	-	PA12	ADC_IN5/USART_RX	I2C_SDA_2
-	-	-	11	PA13	I/O/A	-	PA13	ADC_IN6/I2C_SCL/ USART_CTS	
5	8	7	12	PA4	I/O	LV/PD	PA4	ADC_ETR/TIM1_CH3N	TIM2_CH2_1/TIM2_CH2_3
-	9	8	13	PA5	I/O	LV/PD	PA5	TIM2_CH1	-
6	10	9	14	PA6	I/O/A	-	PA6	ADC_IN0/RST	ISP_1
7	11	10	15	PA7	I/O/A	-	PA7	ADC_IN1/TIM2_CH1N	TIM2_CH1N_1/QII_1
-	-	-	16	PA8	I/O/A	-	PA8	ADC_IN2/TIM2_CH2N	TIM2_CH2N_1
8	12	11	17	PB8	I/O/A	-	PB8	ADC_IN9/QII	-
9	13	12	18	PB7	I/O/A	-	PB7	ADC_IN7/ISN/MCO	-
10	14	13	19	ISP(5)	A	-	ISP	ADC_IN8	-
-	-	-	20	PA14	I/O	-	PA14	USART_RTS/I2C_SDA	-
-	-	-	21	PA15	I/O	-	PA15	TIM1_BKIN	ADC_ETR_1
12	15	15	22	PB0(4)	I/O/A	Rd	PB0	ADC_IN10/SWIO/CC1R	USART_RX_1
11	16	14	23	PA0	I/O/A	-	PA0	ADC_IN12/UDP	USART_TX_2/USART_RX_3
13	17	16	24	PA1	I/O/A	-	PA1	ADC_IN13/UDM	USART_TX_3/USART_RX_2
14	18	17	25	PB1(4)	I/O/A	-	PB1	ADC_IN11/CC2	USART_TX_1
15	19	18	26	PB9(4)	I/O/A	Rd	PB9	ADC_IN14/CC3R/ TIM1_ETR	-
16	20	19	27	V_{DD}	P	-	V_{DD}	-	-

1	1	20	28	PA2	I/O	LV	PA2	TIM1_CH1N	TIM1_CH3_1/I2C_SCL_1/ USART_TX_4

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input, support V_{DD} voltage range input;

O = CMOS level tri-state output, support V_{DD} voltage range input;

P = power supply;

LV= Low voltage driver pins, support input and output of V_{DD} voltage range;

HV= High voltage driver pins, support input and output of V_{HV} voltage range;

PU = Built-in non-closeable pull-up resistor, pull up to V_{HV} voltage, can be used to drive the gate of P-MOSFET;

PD = Built-in pull-down resistor that can be turned off, which is turned on by default and can be used to drive the gate of N-MOSFET;

Rd = Built-in controllable Rd pull-down resistor defined by type-C specification, which can be used in PD receiving end;

A = Analog signal input or output, support V_{DD} voltage range input;

Note 2: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example, TIM2_CH1N_3 indicates that the corresponding bit configuration of the AFIO register is 11b.

Note 3: PB3H and PB4H have built-in pull-up resistors that cannot be closed; PB2H and PB5H have no built-in pull-up resistors; ISP and PB8/QII have no built-in pull-up resistors; PA0 and PA1 have built-in pull-up resistors that can be turned off by default; PB0/CC1R and PB1/CC2/CC2R and PB9/CC3/CC3R have built-in pull-up resistors defined by the type-C specification; in addition, GPIO pins have built-in pull-up resistors that are off by default and can be turned on. PA4 and PA5 have built-in pull-down resistors that can be turned on and off by default; PA0 and PA1 have built-in pull-down resistors that are on, adjustable and off by default, and can provide pull-down current; PB0/CC1R and PB9/CC3R pins have built-in Rd pull-down resistors defined by type-C specification, which are on by default. PB1/CC2 pins do not provide Rd by default and can support customization. Other GPIO pins do not have built-in pull-down resistors. For more details, please refer to the GPIO and its reuse functions section of the CH641RM manual.

Note 4: When PB0, PB1 and PB9 are used as ADC input channels or GPIO push-pull output, the voltage range is about 0V~(V_{DD}-1.7V).

Note 5: The ISP pin feeds the result amplified by the OPA to ADC_IN8.

Note 6: ADC_IN9 is connected to the output terminal of the adjustable gain amplifier QII_OP.

2.3 Pin Alternate Functions

Note that the pin function description in the following table is for all functions and does not involve specific types of chips. There are differences in peripheral resources between different models. Please confirm this function according to the chip model resource table before checking.

Table 2-2 Pin alternate and remapping function

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SWIO	ANA	USB PD
PA0	ADC_IN12			USART_TX_2/USART_RX_3				UDP	
PA1	ADC_IN13			USART_RX_2/USART_TX_3				UDM	
PA2		TIM1_CH1N/TIM1_CH3_1		USART_TX_4		I2C_SCL_1			
PA3		TIM1_CH2N		USART_RX_4		I2C_SDA_1			
PA4	ADC_ETR	TIM1_CH3N	TIM2_CH2_1/TIM2_CH2_3						
PA5			TIM2_CH1						
PA6	ADC_IN0				RST			ISP_1	
PA7	ADC_IN1		TIM2_CH1N/TIM2_CH1N_1					QII_1	
PA8	ADC_IN2		TIM2_CH2N/TIM2_CH2N_1						
PA9			TIM2_CH2/TIM2_CH2_2						
PA10	ADC_IN3								
PA11	ADC_IN4			USART_TX		I2C_SCL_2			
PA12	ADC_IN5			USART_RX		I2C_SDA_2			
PA13	ADC_IN6			USART_CTS		I2C_SCL			
PA14				USART_RTS		I2C_SDA			
PA15	ADC_ETR_1	TIM1_BKIN							
PB0	ADC_IN10			USART_RX_1			SWI0		CC1R
PB1	ADC_IN11			USART_TX_1					CC2
PB2H		TIM1_CH1							
PB3H		TIM1_CH2							

PB4H		TIM1_CH3/TIM1_CH1N_1	TIM2_CH2N_2/TIM2_CH2N_3						
PB5H		TIM1_CH2N_1	TIM2_CH1N_2/TIM2_CH1N_3						
ISP	ADC_IN8							ISP	
PB7	ADC_IN7				MCO			ISN	
PB8	ADC_IN9							QII	
PB9	ADC_IN14	TIM1_ETR							CC3R

Chapter 3 Electrical Characteristics

3.1 Test Conditions

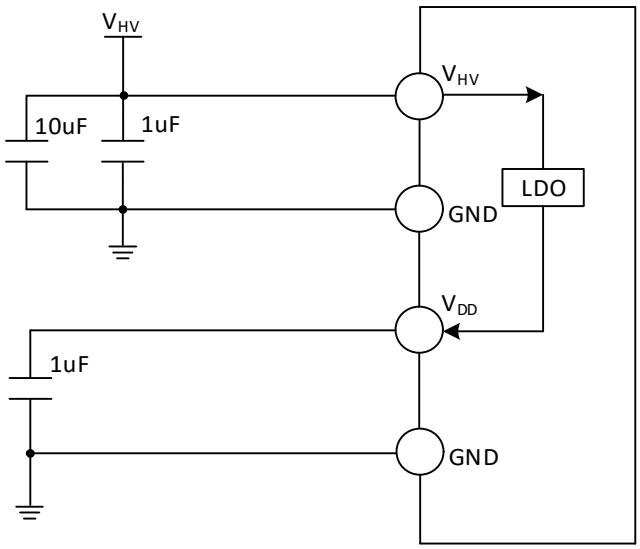
Unless otherwise specified and marked, all voltages are based on GND.

All minimum and maximum values are guaranteed under the worst-case conditions of ambient temperature, supply voltage, and clock frequency. Typical values are provided as design guidelines based on standard operating conditions of 25°C ambient temperature and a supply voltage of V_{HV} = 9V:

Data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained through sample testing. Unless the special instructions are measured, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit of conventional power supply



Note: The V_{DD} pin in the diagram defaults to using an internal voltage regulator with a 1uF capacitor. Alternatively, V_{DD} can be directly supplied from an external source. For detailed information, refer to Section 1.4.3 on power supply options.

3.2 Absolute Maximum Ratings

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Table 3-1 Absolute maximum ratings

Symbol	Description		Min.	Max.	Unit
T_A	Ambient temperature during operation	Rated 5V or 9V, V_{HV} < 10V	-40	85	℃
		Rated 12V, V_{HV} ≥ 10V	-20	70	
T_J	Junction temperature range		-40	105	℃
T_S	Ambient temperature during storage		-40	125	℃

V_{HV}-GND	External main supply voltage (V_{HV})	-0.3	14	V
V_{IN}	Input voltage on HV high voltage pins (PB2H, PB3H, PB4H, PB5H)	-0.3	V_{HV}+0.3	V
	Input voltage on other pins	-0.3	V_{DD}+0.3	V
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (mannequin, non-contact)	2K		V
I_{VHV}	Total current through the V_{DD} power cord (supply current)		200	mA
I_{GND}	Total current passing through the GND ground wire (outflow current)		200	
I_{IO}	Sink current or source current on the HV drive and LV strong drive I/O pin		+/-70	
	Sink current or source current on other common I/O pins		+/-30	
$I_{INJ(PIN)}$	RST pin injection current		+/-4	
	Injection current of other pins		+/-4	
$\sum I_{INJ(PIN)}$	Total injection current of all IO and control pins		+/-20	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HCLK}	Internal HB clock frequency				48	MHz
V_{HV}	Operating power supply voltage	V_{DD} is supplied by an internal voltage regulator	4.0		12.6	V
		V_{DD} is supplied directly from an external power, 3.5V ≤ V_{DD} ≤ 4.8V, V_{HV} is shorted to V_{DD}.	3.5(1)		4.8	V
		V_{DD} is supplied directly from an external power, 4.8V < V_{DD} ≤ 5.5V	V_{DD}		12.6	V
V_{DD}	Internal power supply voltage	VDD is supplied directly from an external power	3.5	5.0	5.5	V
		V_{DD} is supplied by an internal voltage regulator, 4.0V≤ V_{HV} <5.0V	V_{HV}-0.3		V_{HV}	V
		V_{DD} is supplied by an internal voltage regulator, 5.0V≤ V_{HV} ≤12.6V		4.8		V

Note: 1. Actual testing shows that when V_{DD} = 3.2V, the chip can still operate in a basic manner; however, analog functionality will gradually deteriorate as V_{DD} decreases.

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rising rate		3	∞	us/V
	V_{DD} falling rate		3	∞	
t_{VHV}	V_{HV} rising rate		3	∞	us/V
	V_{HV} falling rate		3	∞	

3.3.2 Built-in Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitoring (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Internal voltage regulator output, I/O voltage	V_{HV} > 5V, load < 20mA	4.7	4.8	4.9	V
I_{DD}	External load capacity of VDD	V_{HV} > 5V			15	mA
V_{33}	Internal voltage regulator output, ADC reference	V_{HV} > 8V, V_{DD} > 6V	3.24	3.3	3.36	V
V_{PVD}(1)	Level selection of Programmable Voltage detector	PLS [2:0] = 000 (Rising edge)		3.16		V
		PLS [2:0] = 000 (Falling edge)		2.94		V
		PLS [2:0] = 001 (Rising edge)		3.38		V
		PLS [2:0] = 001 (Falling edge)		3.12		V
		PLS [2:0] = 010 (Rising edge)		3.61		V
		PLS [2:0] = 010 (Falling edge)		3.32		V
		PLS [2:0] = 011 (Rising edge)		3.85		V
		PLS [2:0] = 011 (Falling edge)		3.51		V
		PLS [2:0] = 100 (Rising edge)		4.06		V
		PLS [2:0] = 100 (Falling edge)		3.7		V
		PLS [2:0] = 101 (Rising edge)		4.28		V
		PLS [2:0] = 101 (Falling edge)		3.92		V
		PLS [2:0] = 110 (Rising edge)		4.45		V
		PLS [2:0] = 110 (Falling edge)		4.09		V
		PLS [2:0] = 111 (Rising edge)		4.63		V
		PLS [2:0] = 111 (Falling edge)		4.28		V
$V_{PVDhyst}$	PVD hysteresis		0.18	0.25	0.36	V
$V_{POR/PDR}$	Power-on / power-down reset threshold	Rising edge	2.85	3.00	3.15	V
	V_{HV} undervoltage reset threshold	Falling edge	2.82	2.98	3.12	V
$V_{PDRhyst}$	PDR hysteresis			15	25	mV
V_{OVP}	V_{HV} threshold of OVP reset		13.6	14.3	15	V
T_{OTP}	Temperature point of OTP	Heating process	110	130	150	℃

	The temperature point at which overtemperature protection is removed.	Cooling process	65	85	110	℃
t_{RST}	Power-on reset delay		1	1.5(2)	4	mS
	Other reset delay			300		uS

Note: 1. Normal temperature test value.

2. The user-configurable bit RST_MODE can increase the power-on reset delay.

3.3.3 Built-in Reference Voltage

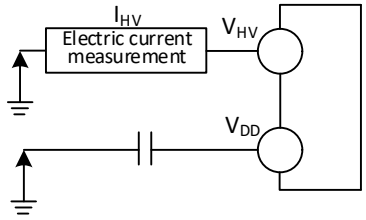
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Built-in reference voltage	T_A = -40℃~85℃	1.18	1.2	1.22	V
$T_{S\_vrefint}$	Sampling time of ADC when internal reference voltage is read out		3		500	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors, including operating voltage, ambient temperature, load of I/O pin, software configuration, operating frequency, flipping rate of I/O pin, location of program in memory and code executed, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

In the case of V_{HV}=9V (V_{DD}=4.8V) at room temperature, during the test: the I/O port that supports pull-up input is configured to pull-up input mode, and the other configuration is analog input mode. HIS = 24M (calibrated); when FHCLK > 24M, the system clock source is PLL. Enable or turn off the power consumption of all peripheral clocks.

Table 3-6 Typical current consumption in Run mode, the data processing code runs from the internal Flash

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{HV}	Supply current in Run mode	Runs on the high-speed internal RC oscillator (HSI).	F_{HCLK} = 48MHz	6.7	4.6	mA
			F_{HCLK} = 24MHz	5.1	4.1	
			F_{HCLK} = 8MHz	3.0	2.7	

		Uses HB prescaler to reduce the frequency.	F_{HCLK} = 4MHz	2.2	2.0	

Note: The above are measured parameters.

Table 3-7 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{HV}	Current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed internal RC oscillator (HSI). Uses HB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	3.7	1.6	mA
			F_{HCLK} = 24MHz	2.1	1.1	
			F_{HCLK} = 8MHz	1.0	0.7	
			F_{HCLK} = 4MHz	0.8	0.6	

Note: The above are measured parameters.

Table 3-8 Typical current consumption in Standby mode

Symbol	Parameter	Condition	Typ.	Unit
I_{HV}	Current in Standby mode	LSI on	64	uA
		LSI off	62	

Note: The above are measured parameters.

3.3.5 Internal Clock Source Characteristics

Table 3-9 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			24		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0℃~70℃	-1.5		1.8	%
		TA = -40℃~85℃	-2.3		2.3	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			10		us
$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Table 3-10 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		100	400	700	KHz
$DuTy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time			80		us

$I_{DD(LSI)}$	LSI oscillator power consumption			2		uA

3.3.6 Wakeup Time from Low-power Mode

Table 3-11 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using the HSI RC clock	22	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stable time + HSI RC clock Wake up	250	us

3.3.7 Memory Characteristics

Table 3-12 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ERASE_64}	Page (64 bytes) programming time	T_A = -20℃~85℃	2.4		3.2	ms
t_{ERASE}	Page (64 bytes) erase time	T_A = -20℃~85℃	2.4		3.2	ms
t_{prog}	16-bit programming time	T_A = -20℃~85℃	2.4		3.2	ms
t_{ME}	Whole piece erasing time	T_A = -20℃~85℃	2.4		3.2	ms
V_{prog}	Programming voltage		3.0		5.3	V

Table 3-13 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase time	T_A = 25℃	10K	80K(1)		Times
t_{RET}	Data retention period		10			Years

Note: 1. Actual number of operational erasures, not guaranteed.

3.3.8 I/O Port Characteristics

Table 3-14 General-purpose I/O and LV strong drive I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage		3.5	4.8	5.5	V
V_{IH}	I/O pin input high voltage	V_{DD} = 3.5V	1.8		V_{DD}	V
		V_{DD} = 4.8V	2.3		V_{DD}	
V_{IL}	I/O pin input low voltage	V_{DD} = 3.5V	0		0.8	V
		V_{DD} = 4.8V	0		1.1	
V_{hys}	Schmitt trigger hysteresis voltage	V_{DD} = 3.5V		220		mV
		V_{DD} = 4.8V		380		
I_{lkg}	Input leakage current of I/O pin			0	+/-3	uA
R_{PU}	Pull-up equivalent resistance		30	45	60	kΩ
R_{PD}	Pull-down equivalent resistance		30	45	60	kΩ
C_{IO}	I/O pin capacitance			5		pF

Table 3-15 General-purpose I/O output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SINK}	Pin output low-level sink current	V_{DD} = 4.8V, pin voltage = 0.4V	12	18	25	mA
I_{SOURCE}	Pin output high-level source current	V_{DD} = 4.8V, pin voltage = V_{DD}-0.4V	11	16	22	mA

Table 3-16 General-purpose I/O output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, single pin absorbs 8mA current	3.5V≤ V_{DD} ≤5V		0.5	V
V_{OH}	Output high level, single pin output 8mA current	3.5V≤ V_{DD} ≤5V	V_{DD}-0.5		V

Note: 1. When PB0, PB1, and PB9 output a high level, the voltage fails to reach full VDD, remaining approximately VDD-1.7V.

2. If multiple IO pins are driven at the same time in the above conditions, the sum of the current must not exceed the absolute maximum rating given in Section 3.2 of the table. When multiple IO pins are driven at the same time, the current on the power / ground pin is large, which will cause a voltage drop so that the voltage of the internal I/O cannot reach the power supply voltage of the meter, resulting in the driving current less than the nominal value.

Table 3-17 General-purpose I/O input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{max(IO)o}$	I/O pin output maximum frequency	CL = 50pF, 3.5V≤ V_{DD} ≤5V		30	MHz
$t_{f(IO)out}$	Falling time of output from high to low level	CL = 50pF, 3.5V≤ V_{DD} ≤5V		12	ns
$t_{r(IO)out}$	Rising time of output from low to high level			12	ns
t_{EXTIpw}	EXTI controller detects the pulse width of the external signal		12		ns

3.3.9 LV Strong Drive I/O Pin Characteristics

Table 3-18 Static characteristics of LV strong-drive I/O pins, refer to Table 3-14

Table 3-19 LV strong drive I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{LSINK}	Pin outputs low-level sink current	V_{DD} = 4.8V, pin voltage = 0.5V	50	65	85	mA
	Pin outputs low-level short-circuit current	V_{DD} = 4.8V, pin voltage = V_{DD}		120		mA
$I_{LSOURCE}$	Pin outputs high-level source current	V_{DD} = 4.8V, pin voltage = V_{DD}-0.5V	30	45	65	mA
	Pin outputs high-level short-circuit current	V_{DD} = 4.8V, pin voltage = 0		115		mA

Table 3-20 LV strong drive I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{LOL}	Output low level, single pin absorbs 30mA current	4V≤ V_{DD} ≤5V		0.5	V
V_{LOH}	Output high level, single pin output 25mA current	4V≤ V_{DD} ≤5V	V_{DD}-0.5		V

Note: If multiple IO pins are driven at the same time in the above conditions, the sum of the current must not exceed the absolute maximum rating given in Section 3.2 of the table. When multiple IO pins are driven at the same time, the current on the power / ground pin is large, which will cause a voltage drop so that the voltage of the internal IBO cannot reach the power supply voltage of the meter, resulting in the driving current less than the nominal value.

Table 3-21 LV strong drive I/O pin input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{Lmax(IO)o}$	I/O pin output maximum frequency	CL = 1000pF, 3.5V≤ V_{DD} ≤5V		3	MHz
$t_{Lf(IO)out}$	Falling time of output from high to low level	CL = 1000pF, 3.5V≤ V_{DD} ≤5V		90	ns
$t_{Lr(IO)out}$	Rising time of output from low to high level			90	ns
$t_{LEXTIpw}$	EXTI controller detects the pulse width of the external signal		12		ns

3.3.10 HV Drive I/O Pin Characteristics

Table 3-22 HV drive I/O pin static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HV}	HV power supply voltage		4.0	9.0	12.6	V
V_{HIH}	I/O pin input high voltage	V_{DD} = 4.8V	2.6		V_{HV}	V
V_{HIL}	I/O pin input low voltage	V_{DD} = 4.8V	0		1.2	V
V_{Hhys}	Schmitt trigger hysteresis voltage	V_{DD} = 4.8V		550		mV
I_{Hlkg}	Input leakage current of I/O pin			0	+/-10	uA
R_{HPU}	Pull-up equivalent resistance		80	120	170	kΩ
C_{HIO}	I/O pin capacitance			10		pF

Table 3-23-1 CH641F/D HV drive I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{HSINK}	Pin outputs low-level sink current	V_{HV} = 5V, pin voltage = 0.5V	25	35	50	mA
	Pin outputs low-level short-circuit current	V_{HV} = 5V, pin voltage = V_{HV}		110	150	mA
	Pin outputs low-level sink current	V_{HV} = 12V, pin voltage = 0.5V	25	35	50	mA
	Pin outputs low-level short-circuit current	V_{HV} = 12V, pin voltage = V_{HV}		130	180	mA
$I_{HSOURCE}$	Pin outputs high-level source	V_{HV} = 5V, pin voltage =	15	21	30	mA

	current	V_{HV}-0.5V				
	Pin outputs high-level short-circuit current	V_{HV} = 5V, pin voltage = 0		80	110	mA
	Pin outputs high-level source current	V_{HV} = 12V, pin voltage = V_{HV}-0.5V	22	31	44	mA
	Pin outputs high-level short-circuit current	V_{HV} = 12V, pin voltage = 0		180	250	mA

Table 3-23-2 CH641X/P HV drive I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{HSINK}	Pin outputs low-level sink current	V_{HV} = 5V, pin voltage = 0.5V	29	70	95	mA
	Pin outputs low-level short-circuit current	V_{HV} = 5V, pin voltage = V_{HV}		220	290	mA
	Pin outputs low-level sink current	V_{HV} = 12V, pin voltage = 0.5V	29	70	95	mA
	Pin outputs low-level short-circuit current	V_{HV} = 12V, pin voltage = V_{HV}		256	340	mA
$I_{HSOURCE}$	Pin outputs high-level source current	V_{HV} = 5V, pin voltage = V_{HV}-0.5V	17	42	57	mA
	Pin outputs high-level short-circuit current	V_{HV} = 5V, pin voltage = 0		156	210	mA
	Pin outputs high-level source current	V_{HV} = 12V, pin voltage = V_{HV}-0.5V	25	62	84	mA
	Pin outputs high-level short-circuit current	V_{HV} = 12V, pin voltage = 0		340	460	mA

Table 3-24 HV drive I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{HOL}	Output low level, single pin absorbs 25mA current	5V ≤ V_{HV} ≤ 12V		0.5	V
V_{HOH}	Output high level, single pin output 15mA current	5V ≤ V_{HV} ≤ 12V	V_{HV}-0.5		V

Note: If multiple IO pins are driven at the same time in the above conditions, the sum of the current must not exceed the absolute maximum rating given in Section 3.2 of the table. When multiple IO pins are driven at the same time, the current on the power / ground pin is large, which will cause a voltage drop so that the voltage of the internal IBO cannot reach the power supply voltage of the meter, resulting in the driving current less than the nominal value.

Table 3-25 HV drive I/O pin input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{Hmax(IO)o}$	I/O pin output maximum frequency	CL = 1000pF, 5V≤ V_{HV} ≤12V		0.5	MHz
C_{HIOmax}	I/O pin maximum load capacitance			2000	pF
$t_{Hf(IO)out}$	CH641F/D output high to low level fall time	CL = 1000pF, 5V≤ V_{HV} ≤12V		150	ns
	CH641X/P output high to low level fall time			90	
$t_{Hr(IO)out}$	CH641F/D output low to high level rise time			150	
	CH641X/P output low to high level rise time			90	ns
$t_{HEXTIpw}$	EXTI controller detects the pulse width of the external signal		12		ns

3.3.11 BC Interface UDP/UDM Characteristics

Table 3-26 BC interface I/O pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{PU}	BC pin pull-up equivalent resistance	DAC = 100000	20	31	45	kΩ
R_{PD}	BC pin pull-down equivalent resistance	DAC = 100000	20	31	45	kΩ
I_{PU2}	BC pin weak pull-up current	PCS = 10, BC output voltage = 0.6V	7	10	14	uA
I_{PD1}	BC pin weak pull-down current	PCS = 01, BC output voltage = 0.6V	1	2	3	uA
I_{PD3}	BC pin pull-down current	PCS = 11, BC output voltage = 0.6V	55	80	110	uA
ET	DAC total error	V_{DD} = 4.8V		0.2	0.8	LSB
V_{DACmax}	DAC maximum output voltage	V_{DD} = 4.8V, non-resistive loads	4.7	4.725		V
V_{DACmin}	DAC minimum output voltage	V_{DD} = 4.8V, non-resistive loads		0	0.02	V
R_{DAC}	DAC output impedance	V_{DD} = 4.8V, disable DAC buffer	12	15.5	20	kΩ
R_{LOAD}	Resistive load	Enable DAC buffer	10			kΩ
I_{DDDAC}	DAC buffer supply current			135		uA
$V_{DACBmax}$	Maximum output voltage with buffer DAC	V_{DD} = 4.8V, load 10kΩ pull-down	4.6	4.72		V
$V_{DACBmin}$	Minimum output voltage with buffer DAC	V_{DD} = 4.8V, load 10kΩ pull-down		0.005	0. 02	V
		V_{DD} = 4.8V, load 10kΩ pull-up		0.08	0. 15	
tBuf	Output delay of a DAC buffer used as a comparator				400	800

3.3.12 USB PD Interface CC1/CC2/CC3 Characteristics

Table 3-27-1 PD interface I/O pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
tRise	Rising time	Time between 10% and 90% of the range,	300	430	600	ns

		minimum value for no-load conditions.				
tFall	Falling time	Time between 10% and 90% of the range, minimum value for no-load conditions.	300	430	600	ns
vSwing	Output voltage swing (peak-to-peak)		1.00	1.12	1.20	V
zDriver	Output impedance	V_{DD} = 4.8V, PD interface output 1.12V	26		90	Ω

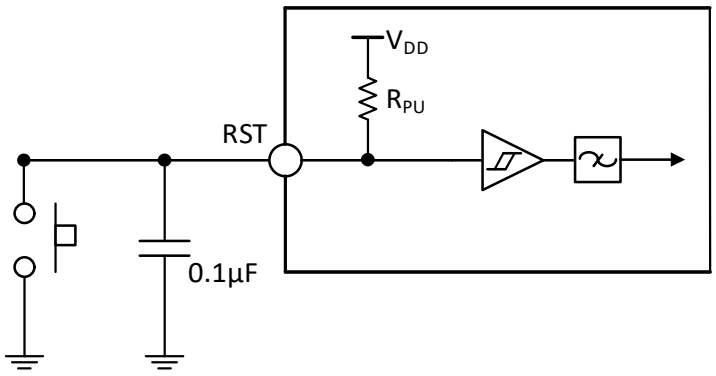
Table 3-27-2 Type-C interface I/O pin characteristics (Voltage value at HVT=0 referenced to common I/O pins)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CCIH}	CC pin input high-level voltage	V_{DD} = 3.5V, HVT = 1	2.1		V_{DD}	V
		V_{DD} = 4.8V, HVT = 1	3.1		V_{DD}	
V_{CCIL}	CC pin input low-level voltage	V_{DD} = 3.5V, HVT = 1	0		1.2	V
		V_{DD} = 4.8V, HVT = 1	0		2.0	
V_{CChys}	Schmitt trigger hysteresis voltage	V_{DD} = 3.5V, HVT = 1	60		450	mV
		V_{DD} = 4.8V, HVT = 1	70		480	
I_{PUCC}	CC pin pull-up current	CC_PU = 11		80±15%		uA
		CC_PU = 10		180±15%		uA
		CC_PU = 01		330±15%		uA
R_{Rd}	CC pin built-in Rd pull-down resistance (Applicable to CC1R/CC2R/CC3R)	CC_PD = 1, V_{DD} ≥ 2.8V or external pull-up 330uA	4.08	5.1	6.12	kΩ
		CC_PD = 0	250	600		kΩ
V_{AINCC}	CC pin ADC conversion voltage range		GND		V_{DD}-1.7	V

3.3.13 RST Pin Characteristics

Circuit reference design and requirements:

Figure 3-3 Typical circuit of external reset pin



Note: The capacitance in the figure is optional and can be used to filter out key jitter.

Table 3-28 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(RST)}$	RST input low-level voltage	V_{DD} = 4.8V	0		1.1	V
$V_{IH(RST)}$	RST input high-level voltage	V_{DD} = 4.8V	2.3		V_{DD}	V

$V_{hys(RST)}$	RST Schmitt trigger hysteresis voltage		150			mV
R_{PU}	Pull-up equivalent resistance		30	45	60	kΩ
$V_{F(RST)}$	RST input can be filtered pulse width				60	ns
$V_{NF(RST)}$	RST input cannot filter pulse width		230			ns

3.3.14 TIM Timer Characteristics

Table 3-29 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns
F_{EXT}	Timer external clock frequency on CH1 to CH3		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.15 I2C Interface Characteristics

Figure 3-4 I2C bus timing diagram

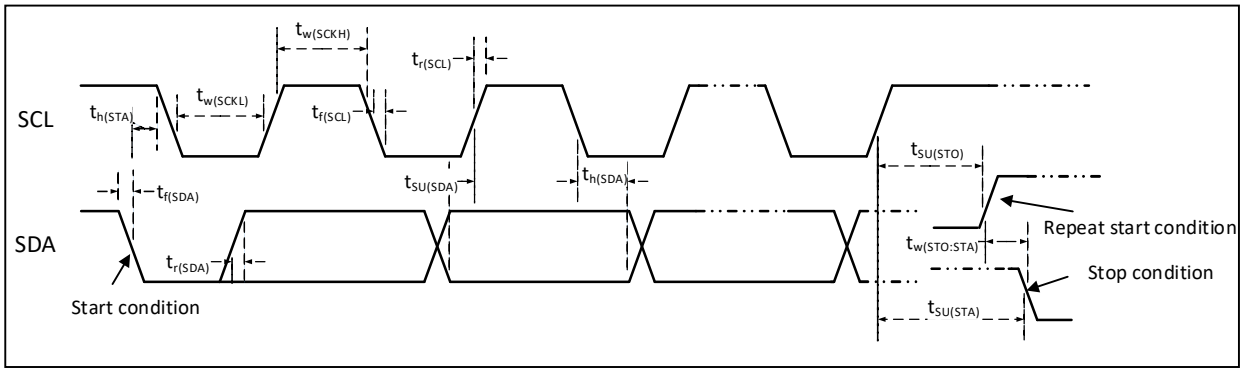


Table 3-30 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns

$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.16 ADC Characteristics

Table 3-31 10-bit ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.5	4.8	5.5	V
I_{DDADC}	Supply current			310		uA
f_{ADC}	ADC clock frequency		2	6	12	MHz
V_{AIN}	Conversion voltage range		GND		V_{33}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
f_S	Sampling rate	f_{ADC} = 2MHz	33		285	KHz
		f_{ADC} = 6MHz	100		430	
		f_{ADC} = 12MHz	200		857	
			1/60		1/14	f_{ADC}
t_s	Sampling time	f_{ADC} = 2MHz	24.5		1.50	us
		f_{ADC} = 6MHz	8.17		0.50	
		f_{ADC} = 12MHz	4.08		0.25	
			49		3	$1/f_{ADC}$
t_{STAB}	Power-on time			7		us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 2MHz	7		30	us
		f_{ADC} = 6MHz	2.33		10	us
		f_{ADC} = 12MHz	1.17		5	us
			14		60	$1/f_{ADC}$

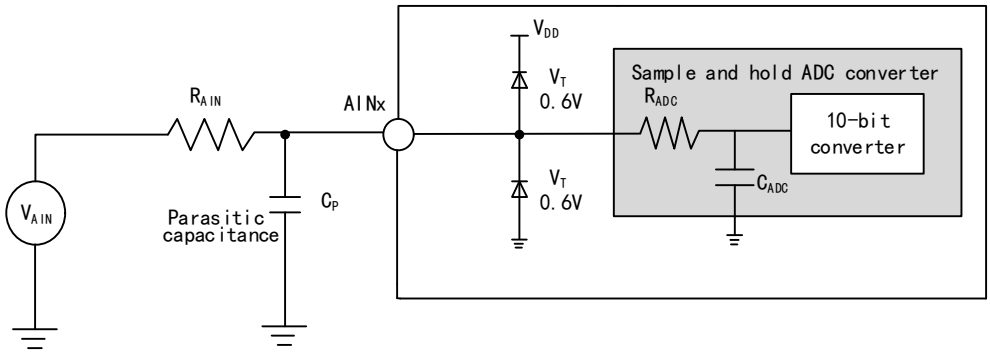
Note: The above are guaranteed design parameters.

Table 3-32 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ET	Total error	f_{ADC} = 12MHz		2	6	LSB
EO	Offset error	f_{ADC} = 12MHz		1	4	
EG	Gain error	f_{ADC} = 12MHz		1	3	
ED	Differential nonlinearity error	f_{ADC} = 12MHz		0.5	2.5	
EL	Integral nonlinearity error	f_{ADC} = 12MHz		0.6	4	

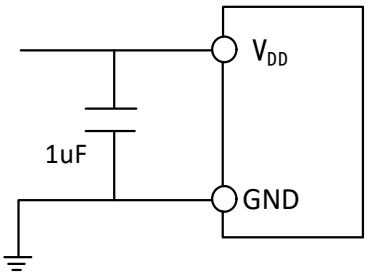
Note: The data in the above table are measured.

Figure 3-5 ADC typical connection diagram



Cp indicates that the PCB and the parasitic capacitance on the pad (about 5pF) may be related to the quality of the pad and PCB layout. A higher Cp value will reduce the conversion accuracy, and the solution is to reduce the FADC value.

Figure 3-6 Analog power supply and decoupling circuit reference



3.3.17 Differential Input Current Sampling ISP/ISN Characteristics

Table 3-33 ISP/ISN differential input current sampling characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage		3.5	4.8	5.5	V
I_{DDISP}	Power supply current			130		uA
V_{BIAS0}	DC bias voltage at ISP pin (external bias recommended)	ISP non-serial resistor	0.27	0.9	1.55	V
$V_{BIAS200}$		ISP external series 200Ω	0.36	1.05	1.76	V
$V_{BIAS500}$		ISP external series 500Ω	0.45	1.3	2.2	V
A_{DC}	DC amplification gain (times)	Single-ended ISP input	70	75	79	V/V
		Differential ISP/ISN input	70	75	79	
$K_{V/A}$	Ratio of output voltage to sampling current	10mΩ sampling differential input	0.70	0.75	0.79	V/A

Note: Measured value.

3.3.18 AC Small Signal Amplifier Decoder QII Characteristics

Table 3-33 AC small signal amplifier decoder characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage		3.5	4.8	5.5	V
I_{DDQII}	Power supply current			220		uA
A_{AC}	Higher gain range for AC amplification	QII_AV = 1，2KHz		23		V/V
	Lower gain range for AC amplification	QII_AV = 0，2KHz		15		
V_{hys}	Comparator hysteresis voltage default value	QII_HYP = 0	150	200	250	mV
	Comparator hysteresis voltage option 2	QII_HYP = 1	60		450	mV
V_{QIIREF}	Reference voltage		1.2	1.5	1.8	V
R_{BIAS}	Bias resistor connected to the reference voltage			185		kΩ

Note: Measured value.

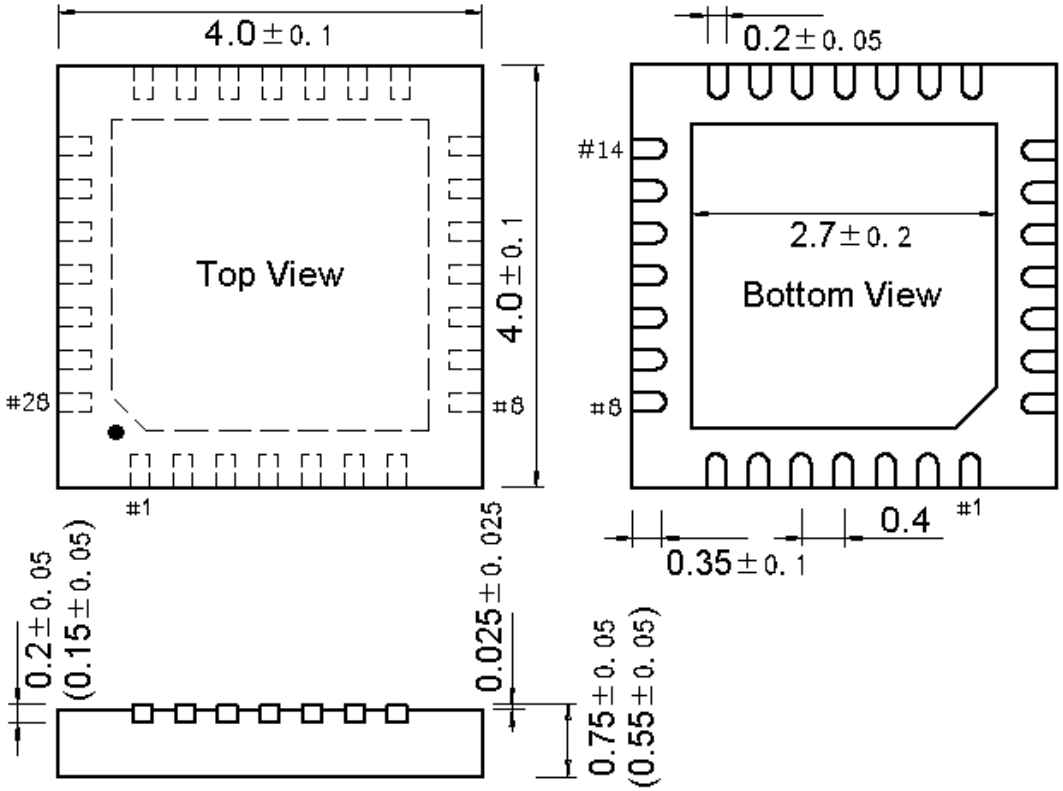
Chapter 4 Package and Ordering Information

Packages

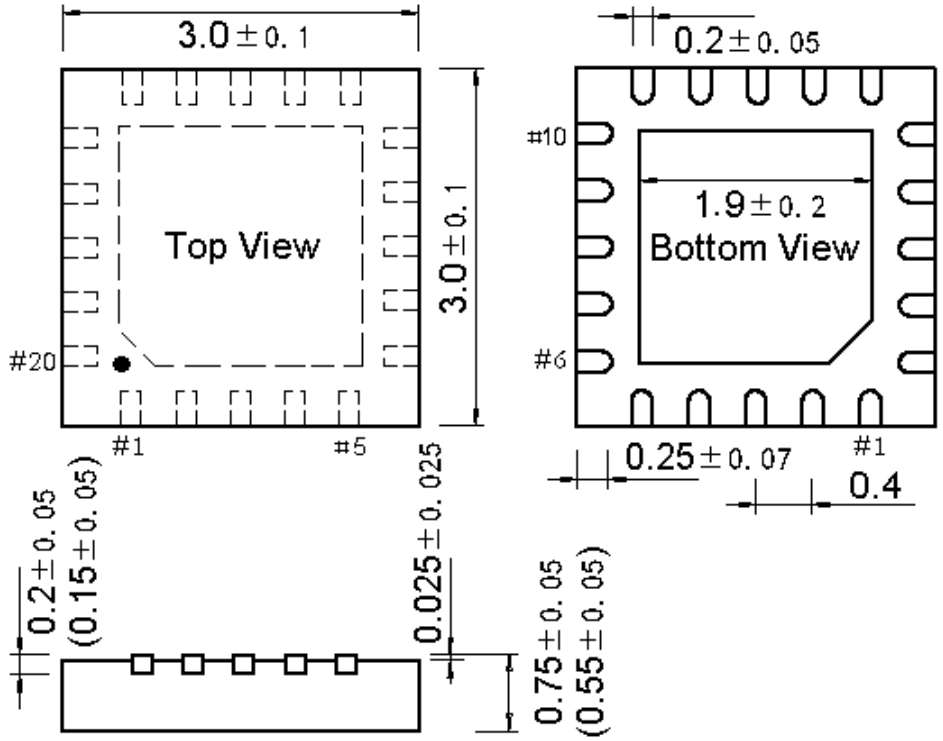
Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN28	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH641F
QFN20	3*3mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH641D
QFN20	3*3mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH641X
QFN16	3*3mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH641P

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

4.1 QFN28 Package



4.2 QFN20 Package



4.3 QFN16 Package