CH32X315/X305 Datasheet

V1.2

Overview

CH32X315 is a multi-channel ADC microcontroller designed based on the QingKe RISC-V core. The core supports 480MHz zero-wait operation and supports single-precision floating point instructions and bit operation instructions. CH32X315 has built-in 4 sets of high-speed 12-bit ADCs, providing 48 direct input channels, supporting scan mode, and can be used with analog switch chips to expand the number of channels to 8 times and automatically switch; It has built-in USB3.0 SuperSpeed controller and PHY, USB2.0 high-speed controller and PHY, and Type-C/PD controller and PHY. It supports USB3.2 Gen1, USBSS Device device function, USBHS Host and USBHS Device function, Type-C and PDUSB fast charging function; it provides DMA controller, ARGB 1-wire RGB driver, multiple sets of timers, 4 sets of USARTs, 2 sets of I2C interfaces, 3 sets of SPI and other rich peripheral resources.

The CH32X305 omits the USB3.0 module found in the CH32X315.

Features

- **Core:**
  - QingKe 32-bit RISC-V3F core, multiple instruction set combinations
  - Fast programmable interrupt controller + hardware interrupt stack
  - 2-level hardware interrupt stack
  - The maximum core frequency is 480MHz and the system maximum frequency is 313MHz
  - In performance mode, the core supports 625MHz and the system supports 400MHz.
- **Memory:**
  - 64KB volatile data storage area SRAM
  - 480KB program memory CodeFlash (192KB Zero-wait application area+288KB non-zero-wait data area)
  - 28KB BootLoader
  - 128B user-defined memory
- **Power management and low-power consumption:**
  - System power supply V_{DD} range: 2.8~3.6V
  - Low-power mode: Sleep, Stop
- **System clock & Reset**
  - Built-in factory-trimmed 20MHz RC oscillator
  - Built-in 40kHz RC oscillator
  - High-speed external 5~32MHz oscillator
  - Power on/down reset, programmable voltage detector
- **Multiple timers**
  - 1×16-bit advanced-control timers, with dead-time control and emergency brake; can offer PWM complementary output for motor control
  - 2×16-bit and 1×32-bit general-purpose timers, providing input capture, output compare, PWM, pulse counting, and incremental encoder input
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 32-bit counter
- **Real-time clock (RTC): 32-bit independent timer**
- **Universal DMA controller:**
  - 11 channels, supports ring buffer management
- **4 sets of 12-bit ADC**
  - Analog input range: V_{REF-}~V_{REF+}
  - 4*12=48 external signals + 1 internal signals
  - Sampling rate up to 5Msps, supports multiple ADC conversion modes
  - Support scanning mode and automatic switching of external extensions
  - Support channel switching in advance to facilitate stable signal sampling
  - Support 4 groups of ADC cascades, equivalent to 20Msps sampling rate
- **4 sets of USART: Support LIN**
- **2 sets of I2C interface**

- **3 sets of SPI interface**
- **5Gbps SuperSpeed USB3.0 controllers and PHY:**
  - Support SuperSpeed Device modes
  - High-speed integrated design, measured 450Mbytes per second
- **480Mbps High-speed USB2.0 controllers and PHY:**
  - Support high-speed/full-speed Host and Device modes
  - Support 1024-byte packets
- **USB PD and Type-C controllers and PHYs:**
  - Support DRP, Sink, and Source applications, as well as PDUSB
  - Support PD3.2 and EPR, with 100W or 240W fast charging
- **Cascadable Addressable Single Wire RGB (ARGB)**
- **Fast GPIO port**
  - 64 I/O ports, mapping 16 external interrupts
- **Security features:** CRC calculation unit, 96-bit chip unique ID
- **Debug mode:** 1-wire/2-wire serial debug interface
- **Package:** LQFP, QFN

Model / Resource difference		CH32X315			CH32X305
		MCU6	WCU6	CCU6	RCT6
Chip pin number		76	68	48	64
Code FLASH (Bytes)		480K(1)	480K(1)	480K(1)	480K(1)
SRAM (Bytes)		64K	64K	64K	64K
GPIO port number		64	59	40	55
Timer	Advanced-control (16-bit)	1	1	1	1
	General-purpose (16-bit)	2	2	2	2
	General-purpose (32-bit)	1	1	1	1
	Watchdog	WWDG+IWDG			WWDG+IWDG
	SysTick (32-bit)	Support			Support
RTC		Support			Support
ADC	ADC1 channel	12+1	12+1	8+1	9+1
	ADC2 channel	12	12	6	10
	ADC3 channel	12	12	8	10
	ADC4 channel	12	12	6	10
USART		4	4	4	4
SPI		3	3	3	3
I2C		2	2	2	2
PDUSB	USBHS(USB2.0)	Host/ Device	Host/ Device	Host/ Device	Host/ Device
	USBSS(USB3.0)	Device	Device	Device	-
	USBPD	1 Built-in Rd(2)	1	1	1
ARGB		1	1	1	1
CPU main frequency		Max: 480MHz			
Operating temperature		Industrial-grade: -40℃~85℃			
Package form		QFN76	QFN68X7	QFN48	LQFP64

Note: 1. The 480KB flash memory contains 192KB of zero-wait program execution area and 288KB of non-zero-wait area.

2. The CH32X315MCU6 chip has a built-in controllable Rd pull-down resistor defined by the Type-C specification, about 5.1kΩ.

Chapter 1 Specification Information

1.1 System Architecture

The microcontroller is based on the RISC-V instruction set architecture (ISA) in which the core, arbitration unit, DMA module, SRAM storage and other parts are interacted through multiple sets of buses. A general-purpose DMA controller is integrated in the chip to reduce the burden on the CPU and improve access efficiency. The application of a multi-level clock management mechanism reduces the operating power consumption of peripherals. At the same time, it has a data protection mechanism and measures such as automatic clock switching protection to increase system stability. The following figure is a block diagram of the overall internal structure of the series of products.

Figure 1-1-1 CH32X315 System block diagram

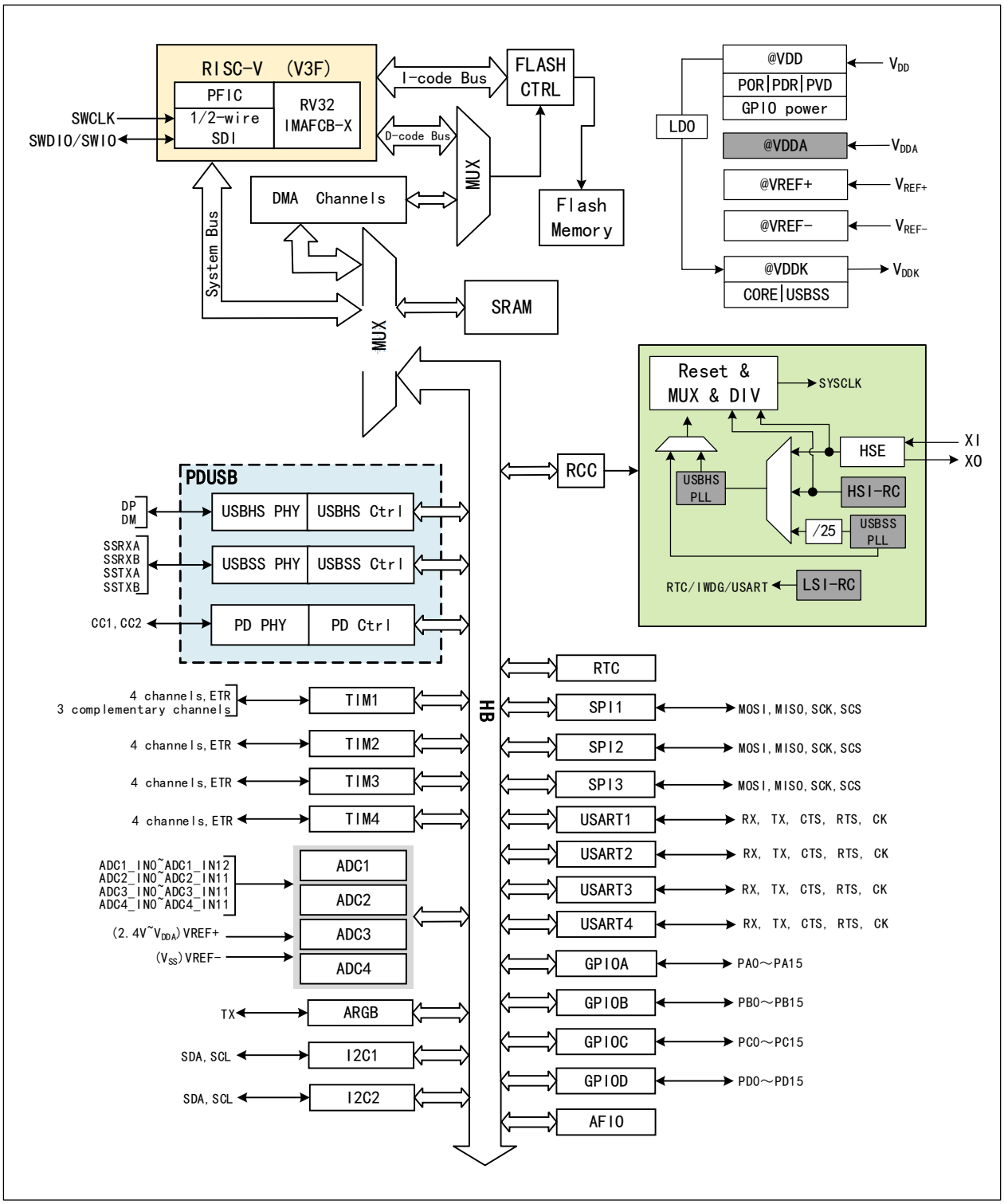
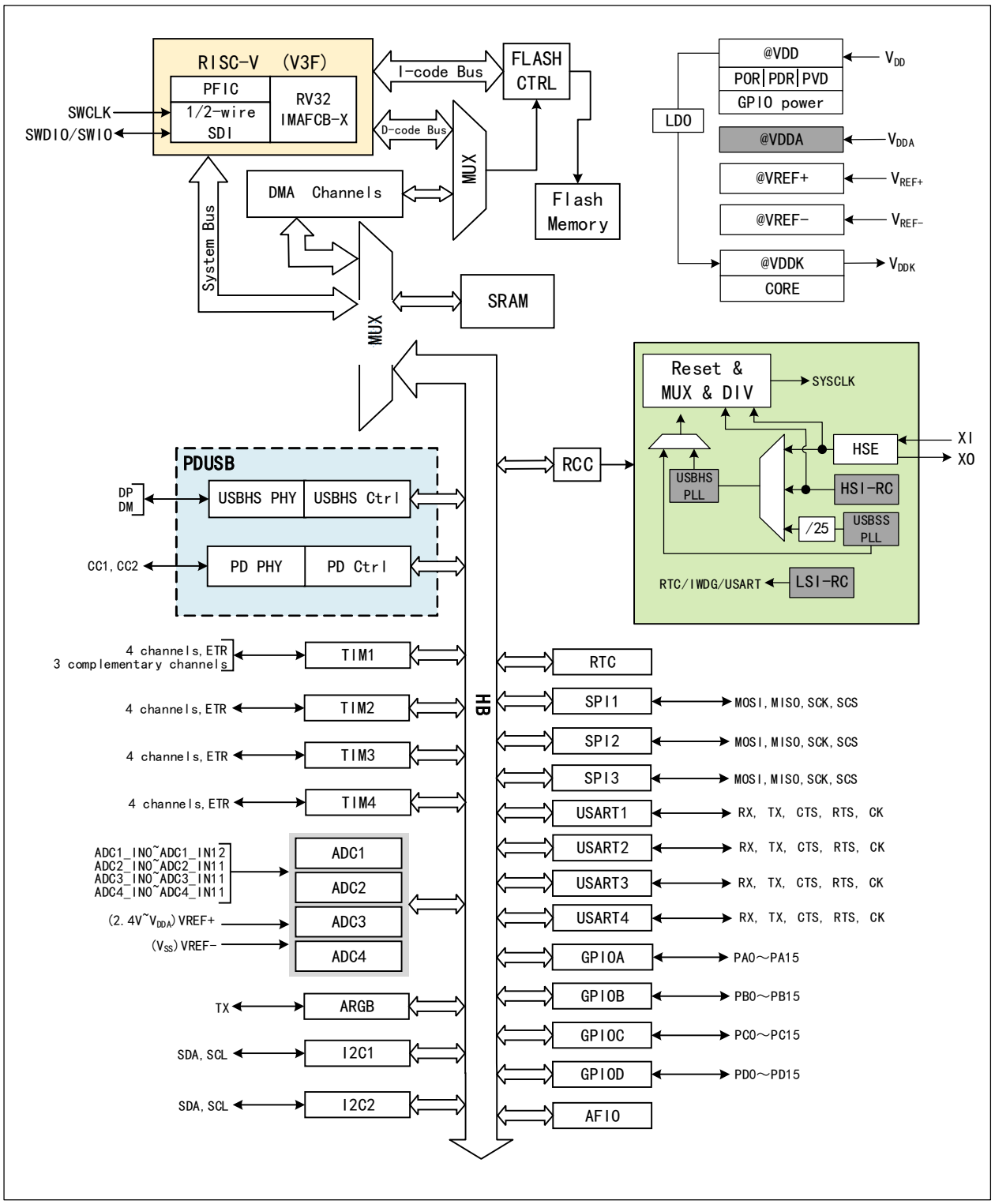
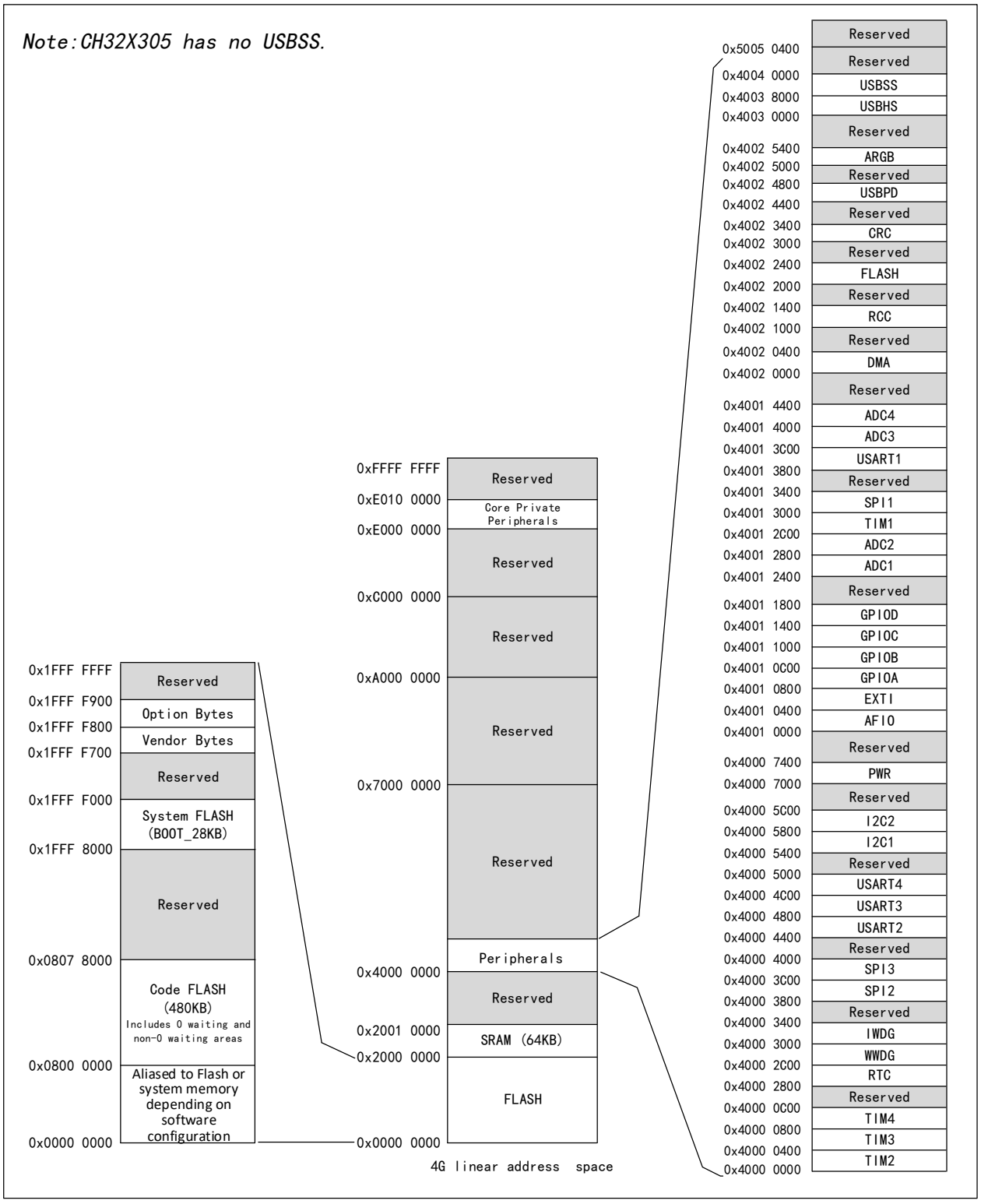


Figure 1-1-2 CH32X305 System block diagram



1.2 Memory Map

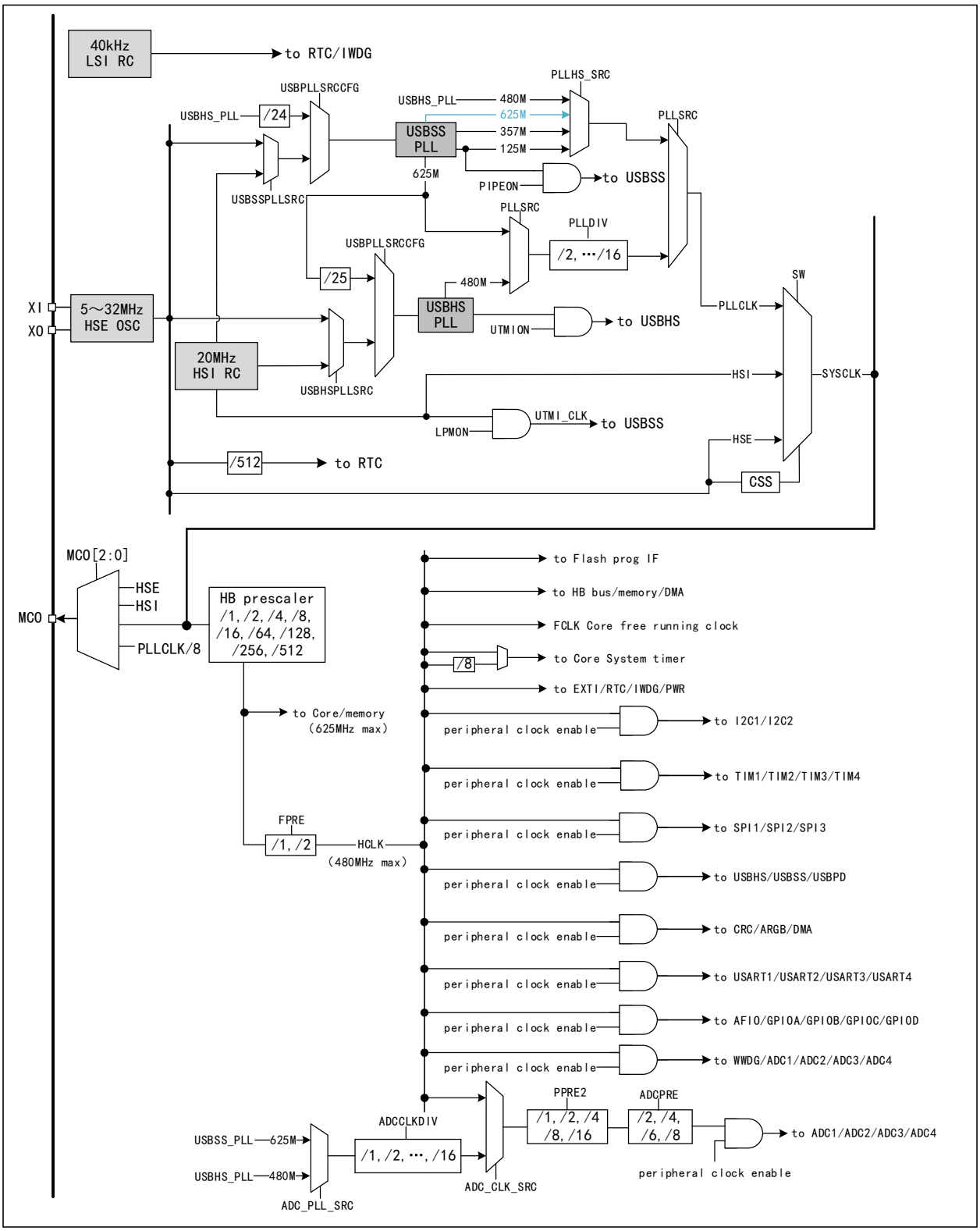
Figure 1-2 Memory address map



1.3 Clock Tree

3 groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), and external high-frequency oscillator (HSE).

Figure 1-3 Clock tree block diagram



Note: The blue marked part in the above picture only applies to chips whose fifth digit of the lot number is greater than 0.

1.4 Functional Description

1.4.1 QingKe RISC-V3F Processor

RISC-V3F supports the RV32IMAFCB-X subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as fast programmable interrupt controller (PFIC) and extended instruction support. Externally multiple buses are connected to external unit modules to enable interaction between external function modules and the core.

With its minimalist instruction set, multiple working modes, and modular customization expansion, QingKe microprocessor can flexibly apply microcontroller design in different scenarios, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc.

- Sequential single-issue architecture
- 3-stage pipeline
- Provide a non-maskable interrupt (NMI)
- 4-channel hardware breakpoints
- 2-level interrupt nesting
- Fast Programmable Interrupt Controller (PFIC)
- Support single-precision floating point instructions
- Support bit operation instructions
- Custom extended instructions
- Hardware interrupt stack

1.4.2 On-chip Memory

Built-in 64K bytes SRAM area for storing data, data will be lost after power failure.

Built-in 480K bytes program flash memory storage area (Code FLASH), i.e. user area, for user's application program and constant data storage. This includes 192K byte zero-wait program area and 288K byte non-zero-wait program execution area.

Built-in 28K bytes System FLASH (System FLASH), i.e. BOOT area, used for system boot program storage, built-in bootstrap loading program.

Built-in 256 bytes system non-volatile configuration information storage area, used for vendor's configuration word storage, factory-cured, user cannot be modified.

Built-in 128 bytes user-defined information storage area for user option byte storage.

1.4.3 Power Supply Scheme

- V_{DD} = 2.8~3.6V: Provides power to I/O pins, system voltage regulator LDO, and built-in USB2.0 PHY. During normal operation, V_{DD} supplies power to the built-in system voltage regulator LDO and outputs regulated power on the V_{DDK} pin. The V_{DD} pin adjacent to the V_{DDK} pin is the main V_{DD}. It is recommended to connect an external high-frequency capacitor of 0.1uF in parallel with a capacity of at least 4.7uF. For other V_{DD}, it is recommended to connect an external high-frequency capacitor of 0.1uF capacity. When used for USB2.0, the V_{DD} range is recommended to be 3.15~3.45V.
- V_{DDA} = 2.8~3.6V: Powers the high-frequency RC oscillator, ADC, and analog portion of the PLL. The V_{DDA} voltage should be the same as the V_{DD} voltage. It is recommended to connect an external high-frequency capacitor with a capacity of 0.1uF.

- V_{REF+} = 2.4~3.6V: For the positive reference voltage of the ADC, it is recommended to connect a nearby 0.01uF high-frequency capacitor in parallel with a 1uF capacity. The V_{REF+} supply voltage must not be higher than the V_{DDA} voltage.
- V_{REF-}= 0~1.0V: For the negative reference voltage of the ADC, it is recommended to short-circuit the system V_{SS}; if a specific negative reference voltage is used, an external 0.01uF high-frequency capacitor with a capacity of 1uF needs to be connected in parallel to V_{SS}.
- V_{DDK} = 1.17~1.27 V: To power the core circuit and the built-in USB3.0PHY, it is recommended to connect an external high-frequency capacitor of 0.1uF in parallel with a capacity of 2.2uF. The cumulative total capacitance does not exceed the total cumulative capacitance of V_{DD}. During normal operation, the V_{DDK} voltage is generated by the system voltage regulator LDO powered by V_{DD}. In order to reduce the self-heating caused by the chip LDO, you can choose an external power supply (can be generated by an external DC-DC). The external power supply voltage is recommended to be slightly higher than the internal LDO output voltage value.

The power pins with the same name above must be short-circuited, and the voltage relationship is: $V_{DD} = V_{DDA}$; and $V_{DDA} \geq V_{REF+}$.

1.4.4 Power Supply Detector

The chip integrates a power-on reset (POR)/power-off reset (PDR) circuit, which is always in a working state; when V_{DD} falls below the set threshold ($V_{POR/PDR}$), it puts the device in reset without the need for an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage magnitude of the V_{DD} supply with the set threshold V_{PVD}. Turning on the corresponding edge interrupt of the PVD allows you to receive an interrupt notification when V_{DD} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for $V_{POR/PDR}$ and V_{PVD} values.

1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are 2 modes of operation depending on the application mode.

- Normal mode: Normal running operation, providing stable core power.
- Low-power mode: After the configuration bit LPDS=1 and the CPU enters stop mode, the voltage regulator can enter a low-power mode, and the core voltage is appropriately reduced at this time.

1.4.6 Low-power Mode

The system supports 2 low-power modes, which can achieve the best balance under the conditions of low-power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

In this mode, the PLL, HSI RC oscillator and HSE crystal oscillator are turned off. Stop mode can achieve the lowest power consumption without losing SRAM and register contents.

The voltage regulator LDO can be entered into a low-power mode from the normal mode through the configuration bit LPDS=1, thereby achieving a lower power consumption state.

Exit condition: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 64 external I/O ports, PVD output, RTC alarm clock, USBPD wake-up signal, USART wake-up signal or USB wake-up signal.

1.4.7 Programmable Fast Interrupt controller (PFIC)

The product has a built-in Programmable Fast Interrupt Controller (PFIC), which supports up to 256 interrupt vectors, and provides flexible interrupt management functions with minimal interrupt latency. The current product manages 7 core private interrupts and 50 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in user and machine privileged modes.

- Support Hardware Interrupt Stack (HPE) without instruction overhead
- Provide 4-channel Vector Table Free Interrupts (VTF)
- Vector table supports address or command mode
- Configurable interrupt nesting depth, up to 2 levels

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 22 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured for its trigger event (rising edge or falling edge or both edges) and can be independently masked; the pending register maintains the status of all interrupt requests. Up to 64 general-purpose I/O ports can be optionally connected to 16 external interrupt lines.

1.4.9 General DMA Controller

The chip has a built-in set of general-purpose DMA controllers that manage 11 channels. The DMA controller can flexibly handle high-speed data transfer from memory to memory, peripheral to memory and memory to peripheral, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: General/advanced/basic TIMx, ADC, USART, I2C, SPI, ARGB.

USBHS, USBSS, and USBPD also have dedicated independent DMA channels.

Note: DMA and CPU access the system SRAM after arbitration by the arbiter.

1.4.10 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 20MHz RC oscillator is used as the default CPU clock, and then an external 5~32MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

1.4.11 Real Time Clock (RTC)

RTC is a set of 32-bit programmable counters, and its time base supports 20-bit prescaler, which is used for long-

time measurement. The clock reference comes from high-speed external clock 512 frequency division (HSE/512) and internal low-power RC oscillator (LSI).

1.4.12 Analog-to-digital Converter (ADC)

The chip has built-in 4 groups of 12-bit high-speed analog/digital converters (ADC1/ADC2/ADC3/ADC4). The 4 groups of ADC provide a total of 4*12=48 external channel samples. ADC1 also provides 1 internal channel (ADC1_IN12). The internal reference voltage V_{REFINT} is connected to the ADC1_IN12 input channel.

The ADC sampling rate can reach 5Msps, supports programmable channel sampling time, can realize single, continuous, scan or intermittent conversion, and supports multiple ADC conversion modes. Providing an analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages. Supports external event-triggered conversion, and trigger sources include internal signals of on-chip timers and external pins. Supports the use of DMA operations.

ADC supports cascade mode. The cascade sequence and the conversion delay of each level of ADC can be configured to achieve simultaneous or sequential delayed conversion; when used in groups, dual ADC mode is supported. In cascade mode, when using 4 groups of ADCs, the trigger delay can be configured to perform alternate sampling. If the trigger delay is 25% of the ADC conversion cycle time, the sampling rate can be increased by 4 times. That is, when 5Msps is used for sampling, the sampling rate can be increased to an equivalent of 20Msps through cascade mode.

ADC contains 2 main steps: signal sampling and A/D analog-to-digital conversion. After the sampling step of the previous channel is completed, the ADC unit of CH32X315/X305 can be set to switch the next channel by hardware in advance. During the A/D conversion process of the previous channel, the next channel completes the process of "switching-switching instant ringing-signal stabilization". This 2-stage pipeline interleaved parallel processing method makes the signal voltage switched in advance stable enough when the next channel is sampled, thereby shortening the sampling time.

ADC supports scan mode. After the scan is completed, the round count can be output through GPIO (ADCS0/PA10, ADCS1/PA11, ADCS2/PA12). In matrix analog signal acquisition applications, the signals generated in this mode can be added with 8-to-1 analog switch chips CH448 to achieve 8 times the number of ADC channels, supporting automatic switching of up to 8*48=384 ADC channels.

The ADC supports low-speed and high-performance modes, with optional 13/14/15-bit modes, that is, 13-bit/14-bit/15-bit conversion results can be obtained in one conversion. After turning on the low-speed high-performance mode, the single ADC conversion cycle (sampling time + conversion time) will increase, that is, 13-bit mode conversion cycle = 12-bit mode conversion cycle * 2, 14-bit mode conversion cycle = 12-bit mode conversion cycle * 4, 15-bit mode conversion cycle = 12-bit mode conversion period * 8.

1.4.13 Timer and Watchdog

The timers in the system include advanced-control timers, general-purpose timers, watchdog timers, and system clock timers.

- Advanced-control timer

The advanced-control timer TIM1 is one 16-bit automatic load increment/decrement counter with 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a 3-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing

the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc.

Advanced-control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer

The general-purpose timer module contains two 16-bit auto-reloadable timers (TIM2 and TIM3) and a 32-bit auto-reloadable timer (TIM4), which are used to measure pulse width or generate pulses of specific frequencies, PWM waves, etc. Can be used in automation control, power supply and other fields.

TIM2/3/4 each have 4 independent channels, each channel supports input capture, output comparison, PWM generation and single pulse mode output. It can also work with advanced timers through the timer link function to provide synchronization or event link functions. In debug mode, the counters can be frozen and the PWM outputs disabled, thereby turning off the switches controlled by these outputs. Any general-purpose timer can be used to generate the PWM output. Each timer has an independent DMA request mechanism.

- Independent watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 40kHz. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window watchdog (WWDG)

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- System time base timer (SysTick)

QingKe microprocessor core comes with a 32-bit optional increment or decrement counter, which is used to generate SYSTICK exceptions, which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, or can be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.14 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 4 sets of Universal Synchronous/Asynchronous Transceivers (USART1/2/3/4). Full-duplex asynchronous communication, synchronous unidirectional communication, and half duplex single line communication are supported, as well as LIN (Local Interconnect Network), and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation for continuous communication.

1.4.15 Serial Peripheral Interface (SPI)

Up to 3 groups of serial peripherals interface provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit selection, hardware CRC

generation/check for reliable communication, and continuous communication support for DMA operation.

1.4.16 I2C Bus

The chip features 2 built-in I2C bus interface capable of operating in either master or slave mode, and supports all I2C-specific timing, protocols, and arbitration. It supports both standard and fast speed.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation.

1.4.17 USB PD and Type-C Controller

The chip has a built-in set of USB Power Delivery controller and PD physical layer transceiver PHY, providing 2 CC pins. Supports USBType-C master-slave detection, automatic BMC codec and CRC, and supports hardware edge control.

Supports USB PD2.0, PD3.0, and PD3.2 power delivery; supports SPR and EPR; supports 100W or 240W high-voltage fast charging; supports PD Sink, PD Source, and DRP applications. Supports PDUSB, UFP, DFP, and DRD applications.

Among them, the CCR in the pins PD4/CC1R and PD5/CC2R of some CH32X315 chips indicates that the CC pin has a built-in controllable Rd pull-down resistor 5K1 defined by the Type-C specification.

1.4.18 Universal Serial Bus USB2.0 High-speed Host/Device Controller (USBHS)

The USB2.0 High-Speed Controller serves dual roles as both a host controller and a device controller. When the USB2.0 high-speed controller is used as a host controller, it can support low-speed, full-speed and high-speed USB devices; when used as a device controller, it can be flexibly set to low-speed, full-speed or high-speed modes to suit various applications. Key features include:

- Support USB2.0, USB1.1, and USB1.0 protocol specifications
- Support USB Host function and USB Device function
- Support control transfers, bulk transfers, interrupt transfers, and real-time/synchronous transfers
- Provide bus reset, suspend, wake-up, and resume functions
- Host supports USB HUB
- All non-zero endpoints support up to 1024-byte packets with built-in FIFO, supporting interrupts and DMA

1.4.19 Universal Serial Bus USB3.0 SuperSpeed Device Controller (USBSS) (Not applicable to CH32X305)

The CH32X315 chip has a built-in USB3.0 SuperSpeed controller and USBPHY physical layer transceiver, which can realize USB3.0 interface product functions and support 5Gbps USBSS SuperSpeed signals.

This controller module provides link layer register access to application code for managing device connections and disconnections, bus status, and power modes. Provides a device (DEVICE) function access interface for implementing various data transmission and upper-layer protocols of the USB3.0 protocol specification. Key features include:

- Support USB3.0 protocol specification and USB3.2 Gen1
- Support USB Device function
- Power management mode supports U1/U2/U3 low power state
- Support control transfers, bulk transfers, interrupt transfers, and real-time/synchronous transfers
- All non-zero endpoints support up to 1024-byte packets, support burst mode

- Support DMA mode to directly access data in each endpoint buffer
- Self-developed controller and transceiver, high-speed integrated design, measured 450Mbytes per second

1.4.20 Cascadable Addressable RGB (ARGB)

The chip incorporates a set of ARGB (Addressable RGB) modules, supporting configurable high and low logic levels for 0-code and 1-code signals, as well as DMA.

The ARGB modules enable timing control for single-data-line RGB light strips and support single-wire RGB daisy-chaining. Compared to traditional RGB, they can drive a wider range of ARGB lighting control ICs, enabling a greater variety of lighting effects.

1.4.21 General-purpose Input and Output (GPIO)

The system provides 4 groups of GPIO ports (PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15) with a total of 64 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port.

All GPIO pins support controllable pull-up and pull-down resistors.

The PD4 and PD5 pins provide pull-up currents that are compatible with USBPD and Type-C specifications and are independently controlled by the PD controller. The PD4/CC1R and PD5/CC2R pins have built-in controllable Rd pull-down resistors defined by the Type-C specification. It is recommended to turn off the pull-down resistors when used as GPIO push-pull outputs.

All I/O pins in the system are powered by V_{DD} rated 3.3V and are shared with digital or analog multiplexing peripherals. Some pins can withstand 5V signal input. By changing the V_{DD} power supply, the high value of the I/O pin output level will be changed to adapt to the external communication interface level.

Provides a locking mechanism to freeze I/O configuration to avoid accidental writes to I/O registers. Please refer to the pin description for specific pins.

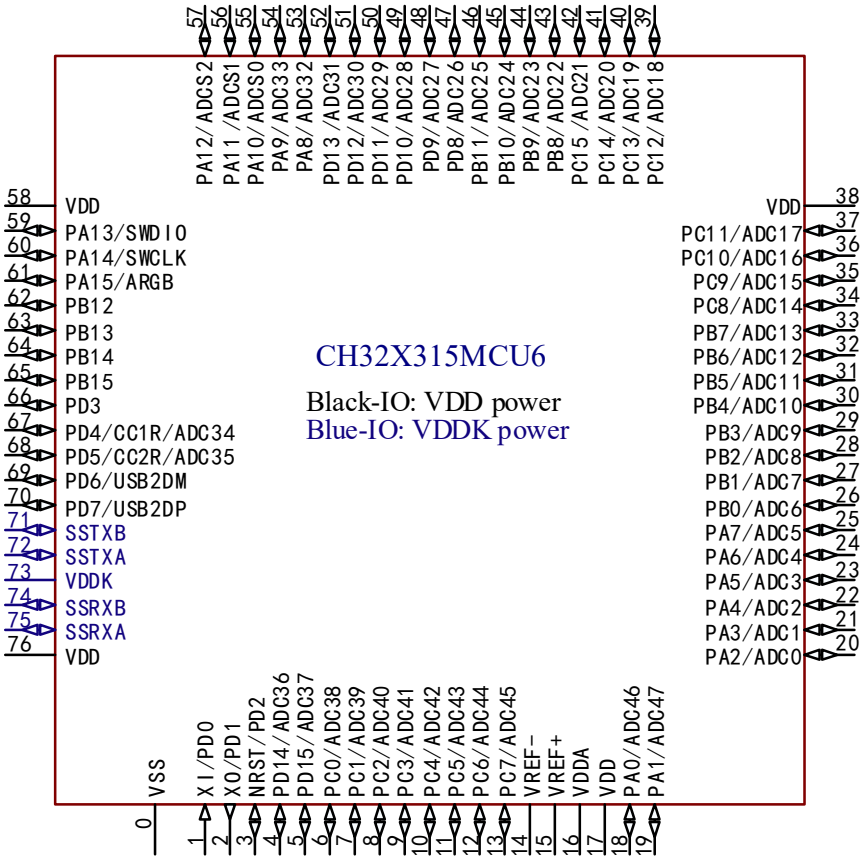
1.4.22 Serial Debug Interface (SDI)

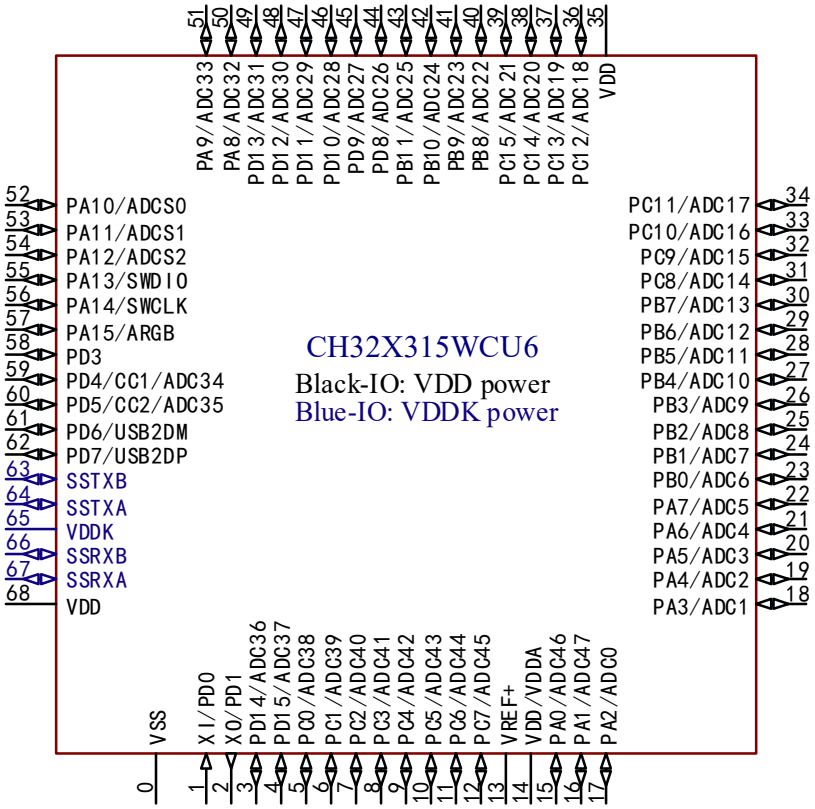
The core includes a built-in 1-wire SDI Serial Debug Interface and a 2-wire SDI Serial Debug Interface. The system supports both 1-wire and 2-wire debug modes. 1-wire debugging is the default mode, utilizing the SWIO pin (Single Wire Input Output). 2-wire debugging employs the SWDIO and SWCLK pins, enhancing download speeds during application. Upon power-up or reset, the debug interface pins default to active functionality. After the main program runs, SDI can be disabled as needed.

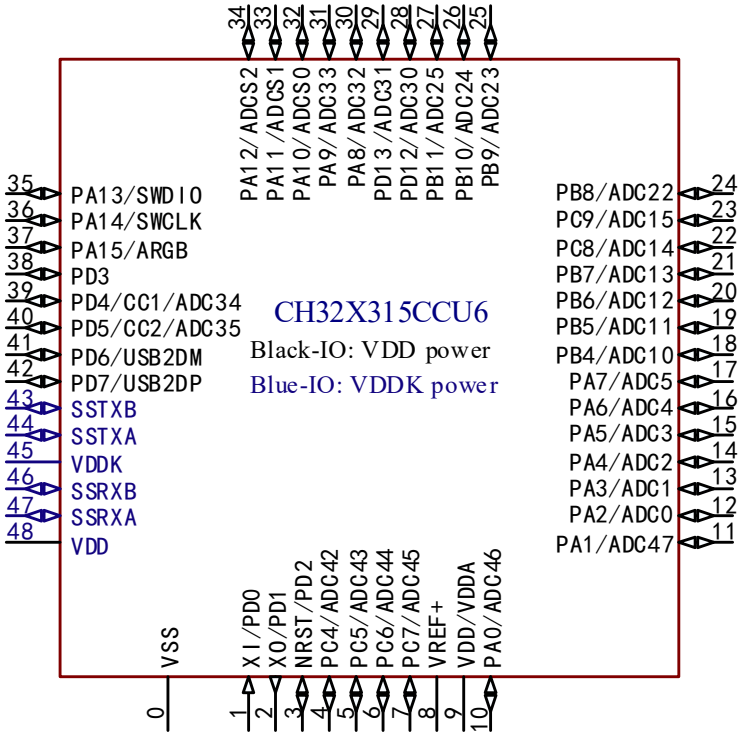
Chapter 2 Pinouts and Pin Definition

2.1 Pinout

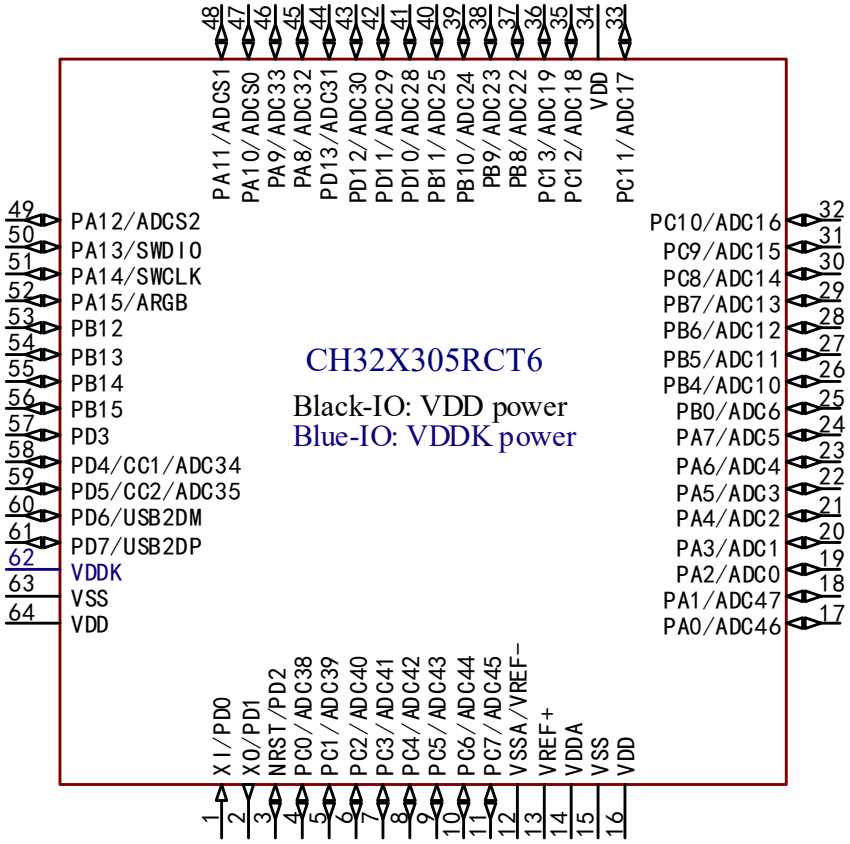
2.1.1 CH32X315 Pinouts







2.1.2 CH32X305 Pinouts



Note: Alternate functions are abbreviated in the pin diagram.

Example:

ADC1_(ADC0: ADC1_IN0, ADC1:ADC1_IN1, ADC2: ADC1_IN2, ADC3: ADC1_IN3, ADC4: ADC1_IN4, ADC5: ADC1_IN5, ADC6:ADC1_IN6, ADC7:ADC1_IN7, ADC8: ADC1_IN8, ADC9: ADC1_IN9, ADC10:

ADC1_IN10, ADC11: ADC1_IN11)
ADC2_(ADC12: ADC2_IN0, ADC13: ADC2_IN1, ADC14: ADC2_IN2, ADC15: ADC2_IN3, ADC16: ADC2_IN4, ADC17:ADC2_IN5, ADC18: ADC2_IN6, ADC19: ADC2_IN7, ADC20: ADC2_IN8, ADC21: ADC2_IN9, ADC22: ADC2_IN10, ADC23: ADC2_IN11)
ADC3_(ADC24: ADC3_IN0, ADC25: ADC3_IN1, ADC26: ADC3_IN2, ADC27: ADC3_IN3, ADC28: ADC3_IN4, ADC29: ADC3_IN5, ADC30: ADC3_IN6, ADC31: ADC3_IN7, ADC32: ADC3_IN8, ADC33: ADC3_IN9, ADC34: ADC3_IN10, ADC35: ADC3_IN11)
ADC4_(ADC36: ADC4_IN0, ADC37: ADC4_IN1, ADC38: ADC4_IN2, ADC39: ADC4_IN3, ADC40: ADC4_IN4, ADC41: ADC4_IN5, ADC42: ADC4_IN6, ADC43: ADC4_IN7, ADC44: ADC4_IN8, ADC45: ADC4_IN9, ADC46: ADC4_IN10, ADC47: ADC4_IN11)
USB2DP: USBHS_DP
USB2DM: USBHS_DM
ARGB: ARGB_TX

2.2 Pin Definitions

Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 2-1-1 CH32X315 pin definitions

Pin No.			Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
CH32X315CCU6	CH32X315WCU6	CH32X315MCU6					
0	0	0	V_{SS}	P	-	V_{SS}	
-	-	-	V_{DD}	P	-	V_{DD}	Main V_{DD}
1	1	1	XI	I/A	-	XI	PD0(2)/USART1_RX(AF1)/I2C2_SCL(AF3)/ SPI1_SCS(AF4)
2	2	2	XO	O/A	-	XO	PD1(2)/USART1_TX(AF1)/I2C2_SDA(AF3)/ SPI1_SCK(AF4)
3	-	3	PD2	I/O	FT	PD2	NRST/SPI1_MOSI(AF4)
-	3	4	PD14	I/O/A	-	PD14	ADC4_IN0/SPI1_MISO(AF4)
-	4	5	PD15	I/O/A	-	PD15	ADC4_IN1
-	5	6	PC0	I/O/A	-	PC0	ADC4_IN2
-	6	7	PC1	I/O/A	-	PC1	ADC4_IN3
-	7	8	PC2	I/O/A	-	PC2	ADC4_IN4
-	8	9	PC3	I/O/A	-	PC3	ADC4_IN5/TIM1_ETR(AF6)/USART1_CK(AF1)
4	9	10	PC4	I/O/A	-	PC4	ADC4_IN6/TIM1_CH1(AF6)/TIM4_CH1(AF 7)/ USART1_TX(AF1)/SPI3_SCS(AF4)
5	10	11	PC5	I/O/A	-	PC5	ADC4_IN7/TIM1_CH2(AF6)/TIM4_CH2(AF 7)/ USART1_RX(AF1)/SPI3_SCK(AF4)
6	11	12	PC6	I/O/A	-	PC6	ADC4_IN8/TIM1_CH3(AF6)/TIM4_CH3(AF 7)/ USART1_CTS(AF1)/SPI3_MOSI(AF4)
7	12	13	PC7	I/O/A	-	PC7	ADC4_IN9/TIM1_CH4(AF6)/TIM4_CH4(AF 7)/ USART1_RTS(AF1)/SPI3_MISO(AF4)
-	-	14	V_{REF-}	P	-	V_{REF-}	
8	13	15	V_{REF+}	P	-	V_{REF+}	
9	14	16	V_{DDA}	P	-	V_{DDA}	
		17	V_{DD}	P	-	V_{DD}	
10	15	18	PA0	I/O/A	-	PA0	ADC4_IN10/TIM1_CH1N(AF6)/

Pin No.			Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
CH32X315CCU6	CH32X315WCU6	CH32X315MCU6					
							TIM4_ETR(AF7)/I2C1_SCL(AF3)
11	16	19	PA1	I/O/A	-	PA1	ADC4_IN11/TIM1_CH2N(AF6)/ I2C1_SDA(AF3)
12	17	20	PA2	I/O/A	-	PA2	ADC1_IN0/TIM1_CH3N(AF6)
13	18	21	PA3	I/O/A	-	PA3	ADC1_IN1/USART2_CK(AF1)
14	19	22	PA4	I/O/A	-	PA4	ADC1_IN2/TIM2_CH1_ETR(AF6)/ USART2_TX(AF1)/SPI1_SCS(AF4)
15	20	23	PA5	I/O/A	-	PA5	ADC1_IN3/TIM2_CH2(AF6)/ USART2_RX(AF1)/SPI1_SCK(AF4)
16	21	24	PA6	I/O/A	-	PA6	ADC1_IN4/TIM2_CH3(AF6)/ USART2_CTS(AF1)/SPI1_MOSI(AF4)
17	22	25	PA7	I/O/A	-	PA7	ADC1_IN5/TIM2_CH4(AF6)/ USART2_RTS(AF1)/SPI1_MISO(AF4)
-	23	26	PB0	I/O/A	-	PB0	ADC1_IN6/SPI1_SCS(AF4)
-	24	27	PB1	I/O/A	-	PB1	ADC1_IN7/SPI1_SCK(AF4)
-	25	28	PB2	I/O/A	-	PB2	ADC1_IN8/SPI1_MOSI(AF4)
-	26	29	PB3	I/O/A	-	PB3	ADC1_IN9/SPI1_MISO(AF4)
18	27	30	PB4	I/O/A	-	PB4	ADC1_IN10/TIM2_CH1_ETR(AF6)/ SPI2_SCS(AF4)
19	28	31	PB5	I/O/A	-	PB5	ADC1_IN11/TIM2_CH2(AF6)/ SPI2_SCK(AF4)
20	29	32	PB6	I/O/A	-	PB6	ADC2_IN0/TIM2_CH3(AF6)/ USART3_CTS(AF1)/SPI2_MOSI(AF4)
21	30	33	PB7	I/O/A	-	PB7	ADC2_IN1/TIM2_CH4(AF6)/ USART3_RTS(AF1)/SPI2_MISO(AF4)
22	31	34	PC8	I/O/A	-	PC8	ADC2_IN2/RTC(AF0)/TIM3_CH1(AF7)/ USART3_TX(AF1)/SPI3_SCS(AF4)
23	32	35	PC9	I/O/A	-	PC9	ADC2_IN3/TIM3_CH2(AF7)/ USART3_RX(AF1)/SPI3_SCK(AF4)
-	33	36	PC10	I/O/A	-	PC10	ADC2_IN4/TIM3_CH3(AF7)/ USART3_CK(AF1)/I2C2_SCL(AF3)/ SPI3_MOSI(AF4)
-	34	37	PC11	I/O/A	-	PC11	ADC2_IN5/TIM3_CH4(AF7)/ I2C2_SDA(AF3)/SPI3_MISO(AF4)
-	35	38	V_{DD}	P	-	V_{DD}	
-	36	39	PC12	I/O/A	-	PC12	ADC2_IN6/TIM3_ETR(AF7)/USART2_TX(AF1)

Pin No.			Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
CH32X315CCU6	CH32X315WCU6	CH32X315MCU6					
-	37	40	PC13	I/O/A	-	PC13	ADC2_IN7/USART2_RX(AF1)
-	38	41	PC14	I/O/A	-	PC14	ADC2_IN8/I2C1_SCL(AF3)
-	39	42	PC15	I/O/A	-	PC15	ADC2_IN9/I2C1_SDA(AF3)
24	40	43	PB8	I/O/A	-	PB8	ADC2_IN10/TIM1_CH1(AF6)
25	41	44	PB9	I/O/A	-	PB9	ADC2_IN11/TIM1_CH2(AF6)/I2C2_SCL(AF3)
26	42	45	PB10	I/O/A	-	PB10	ADC3_IN0/TIM1_CH3(AF6)/I2C2_SDA(AF3)
27	43	46	PB11	I/O/A	-	PB11	ADC3_IN1/TIM1_CH4(AF6)
-	44	47	PD8	I/O/A	-	PD8	ADC3_IN2/USART1_TX(AF1)
-	45	48	PD9	I/O/A	-	PD9	ADC3_IN3/USART1_RX(AF1)
-	46	49	PD10	I/O/A	-	PD10	ADC3_IN4/TIM4_CH1(AF7)/SPI3_SCS(AF4)
-	47	50	PD11	I/O/A	-	PD11	ADC3_IN5/TIM4_CH2(AF7)/ USART4_CK(AF1)/SPI3_SCK(AF4)
28	48	51	PD12	I/O/A	-	PD12	ADC3_IN6/TIM4_CH3(AF7)/ USART4_CTS(AF1)/SPI3_MOSI(AF4)
29	49	52	PD13	I/O/A	-	PD13	ADC3_IN7/TIM1_CH1N(AF6)/ TIM4_CH4(AF7)/USART4_RTS(AF1)/ SPI3_MISO(AF4)
30	50	53	PA8	I/O/A	-	PA8	ADC3_IN8/TIM1_CH2N(AF6)/ USART4_TX(AF1)/I2C1_SCL(AF3)
31	51	54	PA9	I/O/A	-	PA9	ADC3_IN9/TIM1_CH3N(AF6)/ USART4_RX(AF1)/I2C1_SDA(AF3)
32	52	55	PA10	I/O	-	PA10	TIM1_CH1(AF6)/USART1_RX(AF1)/ ADCS0(AF5)
33	53	56	PA11	I/O	-	PA11	TIM1_CH2(AF6)/USART1_TX(AF1)/ I2C2_SCL(AF3)/ADCS1(AF5)
34	54	57	PA12	I/O	-	PA12	TIM1_CH3(AF6)/USART1_RX(AF1)/ I2C2_SDA(AF3)/SPI1_SCS(AF4)/ ADCS2(AF5)
-		58	V_{DD}	P	-	V_{DD}	
35	55	59	PA13	I/O	FT	PA13	SWDIO/SWIO/TIM1_CH1N(AF6)/ USART2_RX(AF2)/USART3_TX(AF1)/ I2C1_SDA(AF3)/SPI1_SCK(AF4)
36	56	60	PA14	I/O	FT	PA14	SWCLK/TIM1_CH2N(AF6)/USART2_TX(AF2)/

Pin No.			Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
CH32X315CCU6	CH32X315WCU6	CH32X315MCU6					
							USART3_RX(AF1)/I2C1_SCL(AF3)/ SPI1_MOSI(AF4)
37	57	61	PA15	I/O	FT	PA15	MCO(AF0)/TIM1_CH3N(AF6)/ TIM3_CH4(AF7)/SPI1_MISO(AF4)/ ARGB_TX(AF5)
-	-	62	PB12	I/O	FT	PB12	USART4_TX(AF1)/SPI2_SCS(AF4)
-	-	63	PB13	I/O	FT	PB13	USART4_RX(AF1)/SPI2_SCK(AF4)
-	-	64	PB14	I/O	FT	PB14	I2C1_SCL(AF3)/SPI2_MOSI(AF4)
-	-	65	PB15	I/O	FT	PB15	I2C1_SDA(AF3)/SPI2_MISO(AF4)
38	58	66	PD3	I/O	FT	PD3	TIM1_BKIN(AF6)/TIM3_CH1(AF7)/ SPI1_MISO(AF4)/ARGB_TX(AF5)
39	59	67	PD4(3)	I/O/A	-	PD4	ADC3_IN10/CC1(AF2)/TIM1_CH4(AF6) TIM3_CH2(AF7)/USART1_TX(AF1)/ I2C1_SCL(AF3)/ARGB_TX(AF5)
40	60	68	PD5(3)	I/O/A	-	PD5	ADC3_IN11/CC2(AF2)/TIM3_CH3(AF7)/ USART1_RX(AF1)/I2C1_SDA(AF3)
41	61	69	PD6	I/O/A	-	PD6	USBHS_DM/USART2_TX(AF1)/I2C2_SCL(AF3)
42	62	70	PD7	I/O/A	-	PD7	USBHS_DP/USART2_RX(AF1)/I2C2_SDA(AF3)
43	63	71	SSTXB	USB	-	SSTXB	
44	64	72	SSTXA	USB	-	SSTXA	
45	65	73	V_{DDK}	P	-	V_{DDK}	
46	66	74	SSRXB	USB	-	SSRXB	
47	67	75	SSRXA	USB	-	SSRXA	
48	68	76	V_{DD}	P	-	V_{DD}	Main V_{DD}

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input; O = CMOS tri-state output; A = Analog signal input or output;

P = Power; USB = USB signal pin; FT = 5V tolerance.

Note 2: For the CH32X315 chip, pins 1 and 2 are configured as XI and XO function pins by default after the chip is reset. The software can reset these 2 pins to PD0 and PD1 functions.

Note 3: In order to reduce the quiescent current of PD4 and PD5, for non-CH32X315MCU6 chips, you can configure PD4 and PD5 as GPIO pull-up, and configure the bits CC1_PD and CC2_PD to 1; you can also configure PD4 and PD5 as GPIO pull-down, and configure the bits CC1_PD and CC2_PD to 0. For the CH32X315MCU6 chip, only PD4 and PD5 can be configured as GPIO pull-downs, and bits CC1_PD and CC2_PD can be configured as 0.

Table 2-1-2 CH32X305 pin definitions

Pin No. CH32X305RCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
1	XI	I/A	-	XI	PD0(2)/USART1_RX(AF1)/I2C2_SCL(AF3)/ SPI1_SCS(AF4)
2	XO	O/A	-	XO	PD1(2)/USART1_TX(AF1)/I2C2_SDA(AF3)/ SPI1_SCK(AF4)
3	PD2	I/O	FT	PD2	NRST/SPI1_MOSI(AF4)
4	PC0	I/O/A	-	PC0	ADC4_IN2
5	PC1	I/O/A	-	PC1	ADC4_IN3
6	PC2	I/O/A	-	PC2	ADC4_IN4
7	PC3	I/O/A	-	PC3	ADC4_IN5/TIM1_ETR(AF6)/USART1_CK(AF1)
8	PC4	I/O/A	-	PC4	ADC4_IN6/TIM1_CH1(AF6)/TIM4_CH1(A F7)/ USART1_TX(AF1)/SPI3_SCS(AF4)
9	PC5	I/O/A	-	PC5	ADC4_IN7/TIM1_CH2(AF6)/TIM4_CH2(A F7)/ USART1_RX(AF1)/SPI3_SCK(AF4)
10	PC6	I/O/A	-	PC6	ADC4_IN8/TIM1_CH3(AF6)/TIM4_CH3(A F7)/ USART1_CTS(AF1)/SPI3_MOSI(AF4)
11	PC7	I/O/A	-	PC7	ADC4_IN9/TIM1_CH4(AF6)/TIM4_CH4(A F7)/ USART1_RTS(AF1)/SPI3_MISO(AF4)
12	V_{REF-}	P	-	V_{REF-}	
	V_{SSA}	P	-	V_{SSA}	
13	V_{REF+}	P	-	V_{REF+}	
14	V_{DDA}	P	-	V_{DDA}	
15	V_{SS}	P	-	V_{SS}	
16	V_{DD}	P	-	V_{DD}	
17	PA0	I/O/A	-	PA0	ADC4_IN10/TIM1_CH1N(AF6)/ TIM4_ETR(AF7)/I2C1_SCL(AF3)
18	PA1	I/O/A	-	PA1	ADC4_IN11/TIM1_CH2N(AF6)/ I2C1_SDA(AF3)
19	PA2	I/O/A	-	PA2	ADC1_IN0/TIM1_CH3N(AF6)
20	PA3	I/O/A	-	PA3	ADC1_IN1/USART2_CK(AF1)

Pin No. CH32X305RCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
21	PA4	I/O/A	-	PA4	ADC1_IN2/TIM2_CH1_ETR(AF6)/ USART2_TX(AF1)/SPI1_SCS(AF4)
22	PA5	I/O/A	-	PA5	ADC1_IN3/TIM2_CH2(AF6)/ USART2_RX(AF1)/SPI1_SCK(AF4)
23	PA6	I/O/A	-	PA6	ADC1_IN4/TIM2_CH3(AF6)/ USART2_CTS(AF1)/SPI1_MOSI(AF4)
24	PA7	I/O/A	-	PA7	ADC1_IN5/TIM2_CH4(AF6)/ USART2_RTS(AF1)/SPI1_MISO(AF4)
25	PB0	I/O/A	-	PB0	ADC1_IN6/SPI1_SCS(AF4)
26	PB4	I/O/A	-	PB4	ADC1_IN10/TIM2_CH1_ETR(AF6)/ SPI2_SCS(AF4)
27	PB5	I/O/A	-	PB5	ADC1_IN11/TIM2_CH2(AF6)/SPI2_SCK(AF4)
28	PB6	I/O/A	-	PB6	ADC2_IN0/TIM2_CH3(AF6)/ USART3_CTS(AF1)/SPI2_MOSI(AF4)
29	PB7	I/O/A	-	PB7	ADC2_IN1/TIM2_CH4(AF6)/ USART3_RTS(AF1)/SPI2_MISO(AF4)
30	PC8	I/O/A	-	PC8	ADC2_IN2/RTC(AF0)/TIM3_CH1(AF7)/ USART3_TX(AF1)/SPI3_SCS(AF4)
31	PC9	I/O/A	-	PC9	ADC2_IN3/TIM3_CH2(AF7)/ USART3_RX(AF1)/SPI3_SCK(AF4)
32	PC10	I/O/A	-	PC10	ADC2_IN4/TIM3_CH3(AF7)/ USART3_CK(AF1)/I2C2_SCL(AF3)/ SPI3_MOSI(AF4)
33	PC11	I/O/A	-	PC11	ADC2_IN5/TIM3_CH4(AF7)/ I2C2_SDA(AF3)/SPI3_MISO(AF4)
34	V_{DD}	P	-	V_{DD}	
35	PC12	I/O/A	-	PC12	ADC2_IN6/TIM3_ETR(AF7)/ USART2_TX(AF1)
36	PC13	I/O/A	-	PC13	ADC2_IN7/USART2_RX(AF1)
37	PB8	I/O/A	-	PB8	ADC2_IN10/TIM1_CH1(AF6)
38	PB9	I/O/A	-	PB9	ADC2_IN11/TIM1_CH2(AF6)/I2C2_SCL(AF3)
39	PB10	I/O/A	-	PB10	ADC3_IN0/TIM1_CH3(AF6)/I2C2_SDA(AF3)
40	PB11	I/O/A	-	PB11	ADC3_IN1/TIM1_CH4(AF6)
41	PD10	I/O/A	-	PD10	ADC3_IN4/TIM4_CH1(AF7)/SPI3_SCS(AF

Pin No. CH32X305RCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
					4)
42	PD11	I/O/A	-	PD11	ADC3_IN5/TIM4_CH2(AF7)/ USART4_CK(AF1)/SPI3_SCK(AF4)
43	PD12	I/O/A	-	PD12	ADC3_IN6/TIM4_CH3(AF7)/ USART4_CTS(AF1)/SPI3_MOSI(AF4)
44	PD13	I/O/A	-	PD13	ADC3_IN7/TIM1_CH1N(AF6)/ TIM4_CH4(AF7)/USART4_RTS(AF1)/ SPI3_MISO(AF4)
45	PA8	I/O/A	-	PA8	ADC3_IN8/TIM1_CH2N(AF6)/ USART4_TX(AF1)/I2C1_SCL(AF3)
46	PA9	I/O/A	-	PA9	ADC3_IN9/TIM1_CH3N(AF6)/ USART4_RX(AF1)/I2C1_SDA(AF3)
47	PA10	I/O	-	PA10	TIM1_CH1(AF6)/USART1_RX(AF1)/ ADCS0(AF5)
48	PA11	I/O	-	PA11	TIM1_CH2(AF6)/USART1_TX(AF1)/ I2C2_SCL(AF3)/ADCS1(AF5)
49	PA12	I/O	-	PA12	TIM1_CH3(AF6)/USART1_RX(AF1)/ I2C2_SDA(AF3)/SPI1_SCS(AF4)/ ADCS2(AF5)
50	PA13	I/O	FT	PA13	SWDIO/SWIO/TIM1_CH1N(AF6)/ USART2_RX(AF2)/USART3_TX(AF1)/ I2C1_SDA(AF3)/SPI1_SCK(AF4)
51	PA14	I/O	FT	PA14	SWCLK/TIM1_CH2N(AF6)/USART2_TX(AF2)/ USART3_RX(AF1)/I2C1_SCL(AF3)/ SPI1_MOSI(AF4)
52	PA15	I/O	FT	PA15	MCO(AF0)/TIM1_CH3N(AF6)/ TIM3_CH4(AF7)/SPI1_MISO(AF4)/ ARGB_TX(AF5)
53	PB12	I/O	FT	PB12	USART4_TX(AF1)/SPI2_SCS(AF4)
54	PB13	I/O	FT	PB13	USART4_RX(AF1)/SPI2_SCK(AF4)
55	PB14	I/O	FT	PB14	I2C1_SCL(AF3)/SPI2_MOSI(AF4)
56	PB15	I/O	FT	PB15	I2C1_SDA(AF3)/SPI2_MISO(AF4)
57	PD3	I/O	FT	PD3	TIM1_BKIN(AF6)/TIM3_CH1(AF7)/ SPI1_MISO(AF4)/ARGB_TX(AF5)
58	PD4(3)	I/O/A	-	PD4	ADC3_IN10/CC1(AF2)/TIM1_CH4(AF6)/ TIM3_CH2(AF7)/USART1_TX(AF1)/

Pin No. CH32X305RCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function
					I2C1_SCL(AF3)/ARGB_TX(AF5)
59	PD5(3)	I/O/A	-	PD5	ADC3_IN11/CC2(AF2)/TIM3_CH3(AF7)/ USART1_RX(AF1)/I2C1_SDA(AF3)
60	PD6	I/O/A	-	PD6	USBHS_DM/USART2_TX(AF1)/I2C2_SCL (AF3)
61	PD7	I/O/A	-	PD7	USBHS_DP/USART2_RX(AF1)/I2C2_SDA(AF3)
62	V_{DDK}	P	-	V_{DDK}	
63	V_{SS}	P	-	V_{SS}	
64	V_{DD}	P	-	V_{DD}	

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input; O = CMOS tri-state output; A = Analog signal input or output; P = Power; FT = 5V tolerance.

Note 2: For the CH32X305 chip, pins 1 and 2 are configured as XI and XO function pins by default after the chip is reset. The software can reset these two pins to PD0 and PD1 functions.

Note 3: In order to reduce the quiescent current of PD4 and PD5, PD4 and PD5 can be configured as GPIO pull-up, and the bits CC1_PD and CC2_PD are configured as 1; PD4 and PD5 can also be configured as GPIO pull-down, and the bits CC1_PD and CC2_PD are configured as 0.

2.3 Pin Alternate Function

Note that the pin function descriptions in the following table are for all functions and do not relate to specific models. There are differences in peripheral resources between different models, please check whether this function is available according to the product model resource table before checking.

Table 2-2-1 ADC Pin Functions

ADC1 function	Default pins
ADC1_IN0	PA2
ADC1_IN1	PA3
ADC1_IN2	PA4
ADC1_IN3	PA5
ADC1_IN4	PA6
ADC1_IN5	PA7
ADC1_IN6	PB0
ADC1_IN7	PB1
ADC1_IN8	PB2
ADC1_IN9	PB3
ADC1_IN10	PB4
ADC1_IN11	PB5
ADC1_IN12	V_{REFINT}
ADC2 function	Default pins
ADC2_IN0	PB6
ADC2_IN1	PB7
ADC2_IN2	PC8
ADC2_IN3	PC9
ADC2_IN4	PC10
ADC2_IN5	PC11
ADC2_IN6	PC12
ADC2_IN7	PC13
ADC2_IN8	PC14
ADC2_IN9	PC15
ADC2_IN10	PB8
ADC2_IN11	PB9
ADC3 function	Default pins
ADC3_IN0	PB10
ADC3_IN1	PB11
ADC3_IN2	PD8
ADC3_IN3	PD9

ADC3_IN4	PD10
ADC3_IN5	PD11
ADC3_IN6	PD12
ADC3_IN7	PD13
ADC3_IN8	PA8
ADC3_IN9	PA9
ADC3_IN10	PD4
ADC3_IN11	PD5
ADC4 function	Default pins
ADC4_IN0	PD14
ADC4_IN1	PD15
ADC4_IN2	PC0
ADC4_IN3	PC1
ADC4_IN4	PC2
ADC4_IN5	PC3
ADC4_IN6	PC4
ADC4_IN7	PC5
ADC4_IN8	PC6
ADC4_IN9	PC7
ADC4_IN10	PA0
ADC4_IN11	PA1
ADC scan function	Optional pins
ADCS0	PA10(AF5)
ADCS1	PA11(AF5)
ADCS2	PA12(AF5)

Table 2-2-2 TIM Pin Functions

TIM1 function	Optional pins
TIM1_ETR	PC3(AF6)
TIM1_CH1	PA10(AF6), PB8(AF6), PC4(AF6)
TIM1_CH2	PA11(AF6), PB9(AF6), PC5(AF6)
TIM1_CH3	PA12(AF6), PB10(AF6), PC6(AF6)
TIM1_CH4	PD4(AF6), PB11(AF6), PC7(AF6)
TIM1_CH1N	PA0(AF6), PA13(AF6), PD13(AF6)
TIM1_CH2N	PA1(AF6), PA8(AF6), PA14(AF6)
TIM1_CH3N	PA2(AF6), PA9(AF6), PA15(AF6)
TIM1_BKIN	PD3(AF6)

TIM2 function	Optional pins
TIM2_CH1_ETR	PA4(AF6), PB4(AF6)
TIM2_CH2	PA5(AF6), PB5(AF6)
TIM2_CH3	PA6(AF6), PB6(AF6)
TIM2_CH4	PA7(AF6), PB7(AF6)
TIM3 function	Optional pins
TIM3_ETR	PC12(AF7)
TIM3_CH1	PC8(AF7), PD3(AF7)
TIM3_CH2	PC9(AF7), PD4(AF7)
TIM3_CH3	PC10(AF7), PD5(AF7)
TIM3_CH4	PC11(AF7), PA15(AF7)
TIM4 function	Optional pins
TIM4_ETR	PA0(AF7)
TIM4_CH1	PC4(AF7), PD10(AF7)
TIM4_CH2	PC5(AF7), PD11(AF7)
TIM4_CH3	PC6(AF7), PD12(AF7)
TIM4_CH4	PC7(AF7), PD13(AF7)

Table 2-2-3 I2C Pin Functions

I2C1 function	Optional pins
I2C1_SCL	PA0(AF3), PA8(AF3), PA14(AF3), PB14(AF3), PC14(AF3), PD4(AF3)
I2C1_SDA	PA1(AF3), PA9(AF3), PA13(AF3), PB15(AF3), PC15(AF3), PD5(AF3)
I2C2 function	Optional pins
I2C2_SCL	PA11(AF3), PB9(AF3), PC10(AF3), PD0(AF3), PD6(AF3)
I2C2_SDA	PA12(AF3), PB10(AF3), PC11(AF3), PD1(AF3), PD7(AF3)

Table 2-2-4 SPI Pin Functions

SPI1 function	Optional pins
SPI1_SCK	PA5(AF4), PA13(AF4), PB1(AF4), PD1(AF4)
SPI1_SCS	PA4(AF4), PA12(AF4), PB0(AF4), PD0(AF4)
SPI1_MOSI	PA6(AF4), PA14(AF4), PB2(AF4) PD2(AF4)
SPI1_MISO	PA7(AF4), PA15(AF4), PB3(AF4), PD3(AF4), PD14(AF4)
SPI2 function	Optional pins
SPI2_SCK	PB5(AF4), PB13(AF4)
SPI2_SCS	PB4(AF4), PB12(AF4)
SPI2_MOSI	PB6(AF4), PB14(AF4)
SPI2_MISO	PB7(AF4), PB15(AF4)
SPI3 function	Optional pins

SPI3_SCK	PC5(AF4), PC9(AF4), PD11(AF4)
SPI3_SCS	PC4(AF4), PC8(AF4), PD10(AF4)
SPI3_MOSI	PC6(AF4), PC10(AF4), PD12(AF4)
SPI3_MISO	PC7(AF4), PC11(AF4), PD13(AF4)

Table 2-2-5 USART Pin Functions

USART1 function	Optional pins
USART1_CK	PC3(AF1)
USART1_RX	PA10(AF1), PA12(AF1), PC5(AF1), PD0(AF1), PD5(AF1), PD9(AF1)
USART1_TX	PA11(AF1), PC4(AF1), PD1(AF1), PD4(AF1), PD8(AF1)
USART1_RTS	PC7(AF1)
USART1_CTS	PC6(AF1)
USART2 function	Optional pins
USART2_CK	PA3(AF1)
USART2_RX	PA5(AF1), PA13(AF2), PC13(AF1), PD7(AF1)
USART2_TX	PA4(AF1), PA14(AF2), PC12(AF1), PD6(AF1)
USART2_RTS	PA7(AF1)
USART2_CTS	PA6(AF1)
USART3 function	Optional pins
USART3_CK	PC10(AF1)
USART3_RX	PA14(AF1), PC9(AF1)
USART3_TX	PA13(AF1), PC8(AF1)
USART3_RTS	PB7(AF1)
USART3_CTS	PB6(AF1)
USART4 function	Optional pins
USART4_CK	PD11(AF1)
USART4_RX	PA9(AF1), PB13(AF1)
USART4_TX	PA8(AF1), PB12(AF1)
USART4_RTS	PD13(AF1)
USART4_CTS	PD12(AF1)

Table 2-2-6 USBPD Pin Functions

USBPD function	Optional pins
CC1	PD4(AF2)
CC2	PD5(AF2)

Table 2-2-7 USBHS Pin Functions

USBHS function	Optional pins
USBHS_DP	PD7
USBHS_DM	PD6

Table 2-2-8 ARGB Pin Functions

ARGB function	Optional pins
ARGB_TX	PA15(AF5), PD3(AF5), PD4(AF5)

Table 2-2-9 Debug Pin Functions

Debug pin function	Default pins
SWCLK	PA14
SWDIO/SWIO	PA13

Table 2-2-10 MCO Pin Functions

MCO function	Optional pins
MCO	PA15(AF0)

Table 2-2-11 RTC Pin Functions

RTC function	Optional pins
RTC	PC8(AF0)

Table 2-2-12 Reset Pin Functions

NRST function	Optional pins
NRST	PD2

Chapter 3 Electrical Characteristics

3.1 Test Conditions

Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency.

Typical values for CH32X315 and CH32X305 are based on one of the following two environments for design guidance:

1. At room temperature of 25°C, power supply V_{DD} = 3.3V, V_{DDA} = 3.3V, V_{REF+} = 3.3V, generate V_{DDK} = 1.2V.
2. At room temperature of 25°C, the external DCDC chip (CH2003K) provides rated 5V, which generates rated 3.3V and 1.2V for supply to CH32X315. Power supply V_{DD} = V_{DDA} = V_{REF+} = 3.3V, V_{DDK} = 1.2V.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1-1 Standard power supply typical circuit

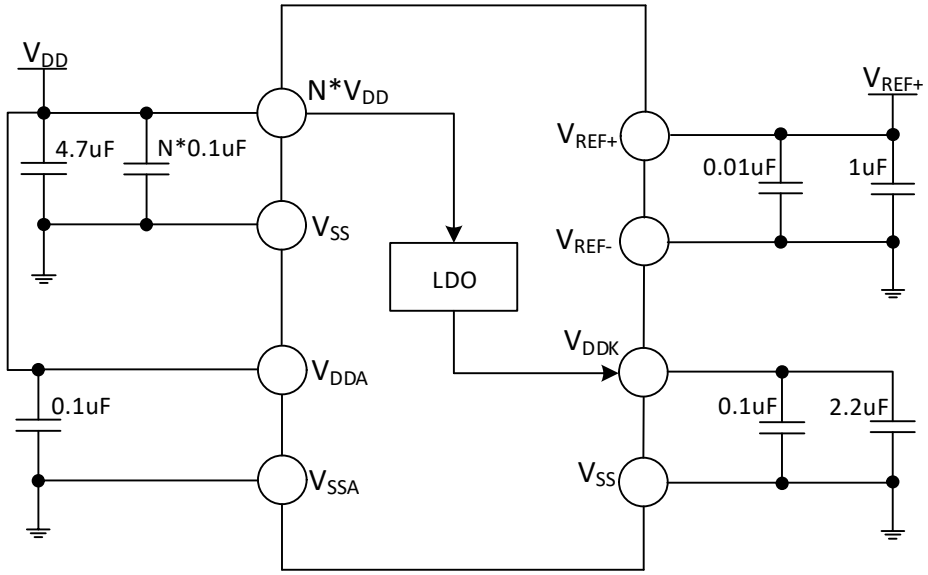
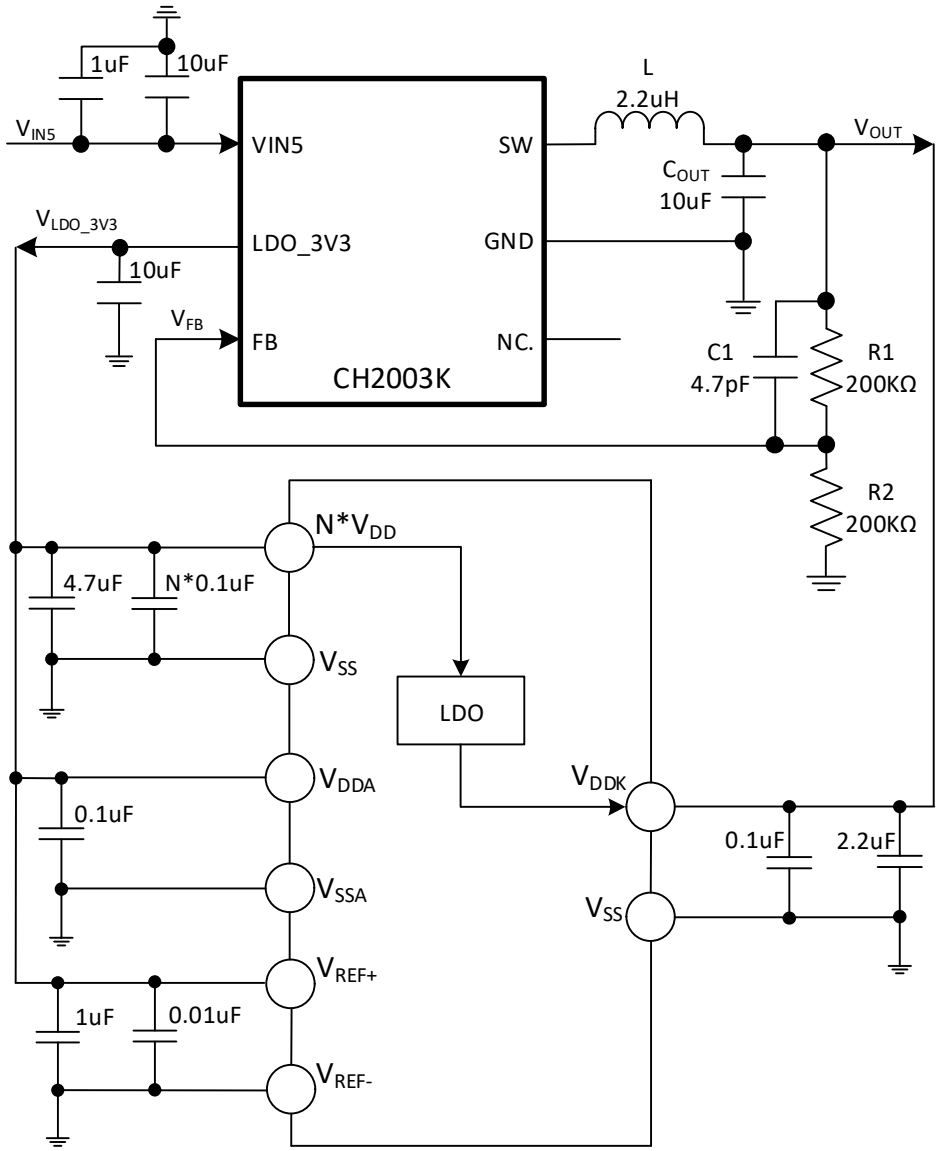


Figure 3-1-2 Typical circuit of conventional single 5V power supply



Note: 1. For CH32X315 and CH32X305 chips, V_{DD} has multiple pins in the chip package, and the power supply pins with the same name must be short-circuited.

2. The main V_{DD} pin (adjacent or close to the V_{DDK} pin) is connected to an external decoupling capacitor of 0.1uF in parallel with a capacity of at least 4.7uF. The remaining V_{DD} pins only need to be connected to an external decoupling capacitor of 0.1uF.

3. For the circuit shown in Figure 3-1-2 above, the bits LDO_VDDK/LDO_VDD12A need to be adjusted down to 010 to give way to the external 1.2V power supply.

3.2 Absolute Maximum Ratings (Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}	External main supply voltage	-0.3	4.0	V

V_{DDA}	Analog part supply voltage		-0.3	4.0	V
V_{DDK}	Core operating voltage, USB3.0 module operating voltage		-0.2	1.4	V
V_{REF+}	Positive reference voltage for ADC module		-0.3	V_{DDA}+0.3	V
V_{REF-}	Negative reference voltage for ADC module		-0.3	1.3	V
V_{IN}	Input voltage on FT (5V tolerant) pin		-0.3	5.5	V
	Input voltage on USB2.0 pin		-0.3	V_{DD}+0.3	V
	Input voltage on USB3.0 pin	CH32X315	-0.3	V_{DDK}+0.3	V
	Input voltage on other I/O pins (V_{DD} supply)		-0.3	V_{DD}+0.3	V
$\|\Delta V_{DD\_x}\|$	Voltage difference between V_{DD} of main power supply pin			20	mV
$\|\Delta V_{SS\_x}\|$	Voltage difference between V_{SS} of common ground pin			20	mV
$V_{ESDIO(HBM)}$	SD electrostatic discharge voltage (HBM) of I/O pin		4K		V
	USB2.0 and USB3.0 pin		4K		V
I_{VDD}	Total current of all V_{DD} main supply pins			250	mA
I_{VSS}	Total current of all V_{SS} common ground pins			250	mA
I_{IO}	Sink current on any I/O and control pin			25	mA
	Source current on any I/O and control pin			-25	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HCLK}	System HB clock frequency	LDO_VDDK = 101 (default)			312.5(3)	MHz
		LDO_VDDK = 111 (Performance mode)			400(5)	MHz
F_{CORE}	Core RISC-V3F frequency	LDO_VDDK = 101 (default)			480(4)	MHz
		LDO_VDDK = 111 (Performance mode)			625(5)	MHz
V_{DD}(6)	Standard working voltage	Not used USB2.0	2.8	3.3	3.6	V
		Use USB2.0	3.15	3.3	3.45	V
V_{DDA}	Analog part working voltage	V_{DDA} should be the same as V_{DD}, V_{REF+} cannot be higher than V_{DDA}, V_{REF-} is recommended to be equal to V_{SS}	2.8	3.3	3.6	V
V_{DDK}(1)	Core operating voltage, USB3.0 module operating voltage		1.17	1.2	1.27	V
V_{REF+}(2)	Positive reference voltage for ADC module	V_{REF+} must not exceed V_{DDA}; V_{REF-} should be equal to V_{SS}.	2.4	3.3	3.6	V
T_A	Ambient temperature during operation		-40		85	℃
T_J	Junction temperature		-40		105	℃

Note: 1. The V_{DDK} current is relatively large. Considering the voltage drop loss of the PCB trace, if the external

power supply is provided, it is recommended to add 1.2V and 10~50mV.

2. The V_{REF+} external capacitor should be as close as possible, otherwise it will affect the ADC performance.

3. Measured at room temperature, the frequency is no less than 480MHz; however, this does not account for temperature and process variations. The use of 480MHz is prohibited in production applications.

4. Measured at room temperature, the frequency is no less than 625MHz; however, this does not account for temperature and process variations. The use of 625MHz is prohibited in production applications.

5. Suitable only for commercial-grade applications: $T_A \leq 70°C$ and with adequate heat dissipation.

6. For V_{DD}, the resistance of the power line should be small enough, and the decoupling capacitor should be placed close to the chip power pin to avoid false triggering of power-on/power-down reset due to the IR voltage drop or transient large current of the power network.

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		20	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Programmable voltage detector level selection	PLS[1:0] = 00 (rising edge)		2.79		V
		PLS[1:0] = 00 (falling edge)		2.77		V
		PLS[1:0] = 01 (rising edge)		2.91		V
		PLS[1:0] = 01 (falling edge)		2.88		V
		PLS[1:0] = 10 (rising edge)		3.01		V
		PLS[1:0] = 10 (falling edge)		2.99		V
		PLS[1:0] = 11 (rising edge)		3.09		V
		PLS[1:0] = 11 (falling edge)		3.07		V
$V_{PVDhyst}$	PVD hysteresis			0.02		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge		2.65		V
		Falling edge		2.64		V
$V_{PDRhyst}$	PDR hysteresis			10		mV
$t_{RSTTEMPO}$	Power on reset		16	28	30	ms
	Other reset		2	20	30	ms

Note: 1. Normal temperature test value.

3.3.3 Built-in Reference Voltage

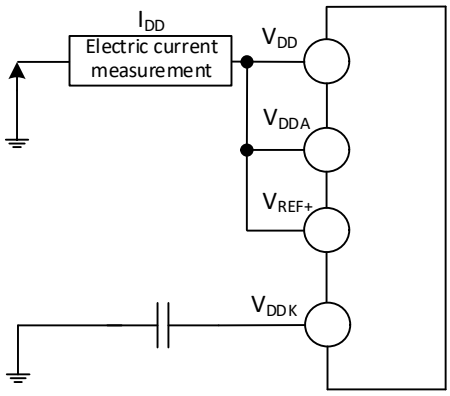
Table 3-5 Built-in reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C	1.17	1.2	1.23	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage		3.6			us

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



CH32X305 and CH32X315 are in the following conditions:

1. Under room temperature conditions (V_{DD} = V_{DDA} = 3.3V, V_{DDK} = 1.2V),
2. At room temperature, the external DCDC chip (CH2003K) provides a rated 5V, which generates a rated 3.3V and 1.2V for the CH32X315 chip.

When testing at the same time: all I/O ports are configured with pull-down inputs, only one HSE or HSI is turned on, HSE=20M, HSI=20M (calibrated). Enables or disables the power consumption of all peripheral clocks.

Table 3-6-1 Typical current consumption in Run mode, data processing code runs from internal flash memory

Symbol	Parameter	Condition			Typ.		Unit
		Clock	F_{CORE}	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	External clock	F_{CORE} = 480MHz(2)	F_{HCLK} = 480MHz(2)	74.8	41.1	mA
			F_{CORE} = 480MHz	F_{HCLK} = 240MHz	51.1	34.8	
			F_{CORE} = 240MHz	F_{HCLK} = 240MHz	38.9	22.5	
			F_{CORE} = 120MHz	F_{HCLK} = 120MHz	22.6	14.4	
			F_{CORE} = 60MHz	F_{HCLK} = 60MHz	14.4	10.4	
			F_{CORE} = 20MHz	F_{HCLK} = 20MHz	5.7	4.3	
		Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the	F_{CORE} = 480MHz	F_{HCLK} = 240MHz	49.9	33.7	
			F_{CORE} = 240MHz	F_{HCLK} = 240MHz	38.2	21.8	
			F_{CORE} = 120MHz	F_{HCLK} = 120MHz	22.1	13.8	
			F_{CORE} = 60MHz	F_{HCLK} = 60MHz	13.8	9.7	
			F_{CORE} = 20MHz	F_{HCLK} = 20MHz	4.9	3.6	

		frequency.					

Note: 1. The above are the measured parameters.

2. Actual measurements were taken under performance mode (where LDO_VDDK = 111).

Table 3-6-2 In Run mode, using USB3.0, typical current consumption increased by V_{DDK}, data processing code runs from SRAM

Symbol	Parameter	Condition	Typ.	Unit
I_{DDK}(1)(2)	In Run mode, V_{DDK} supplies current	Use USB3.0	85	mA

Note: 1. The above are the measured parameters.

2. When V_{DDK} is directly powered from the outside, the power supply capacity of the external power supply must be sufficiently greater than the sum of the values in Table 3-6-1 and Table 3-6-2.

Table 3-7 Typical current consumption in Sleep mode, data processing code runs from internal flash memory or SRAM

Symbol	Parameter	Condition			Typ.		Unit
		Clock	F_{CORE}	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in sleep mode (when peripherals are powered and clocks are maintained)	External clock	F_{CORE} = 480MHz	F_{HCLK} = 240MHz	28.5	12.1	mA
			F_{CORE} = 240MHz	F_{HCLK} = 240MHz	27.9	11.5	
			F_{CORE} = 120MHz	F_{HCLK} = 120MHz	17.1	8.9	
			F_{CORE} = 60MHz	F_{HCLK} = 60MHz	11.7	7.6	
			F_{CORE} = 20MHz	F_{HCLK} = 20MHz	4.7	3.3	
		Run from high-speed internal RC oscillator (HSI), uses HB prescaler to reduce frequency	F_{CORE} = 480MHz	F_{HCLK} = 240MHz	27.8	11.3	
			F_{CORE} = 240MHz	F_{HCLK} = 240MHz	27.2	10.8	
			F_{CORE} = 120MHz	F_{HCLK} = 120MHz	16.5	8.3	
			F_{CORE} = 60MHz	F_{HCLK} = 60MHz	11.1	6.9	
			F_{CORE} = 20MHz	F_{HCLK} = 20MHz	4.0	2.6	

Note: 1. The above are the measured parameters.

Table 3-8 Typical current consumption in Stop mode

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}(1)(2)(3)	Supply current in Stop mode	The regulator is in normal mode, the low-speed and high-speed internal RC oscillators and the external oscillator are off (no independent watchdog)	1.1	mA
		The voltage regulator is in low power mode, the low-speed and high-speed	1.0	

		internal RC oscillators and the external oscillator are off (no independent watchdog, PVD is off)		

Note: 1. The above are measured parameters.

2. In the table above, the test results are based on the conditions where bit PLAN = 1, LDO_VDD12A[2:0] = 011b, and LDO_VDDK[2:0] = 011b.

3. To reduce the static current of PD4 and PD5, for non-CH32X315MCU6 chips, PD4 and PD5 can be configured as GPIO pull-up, with bits CC1_PD and CC2_PD set to 1; alternatively, PD4 and PD5 can be configured as GPIO pull-down, with bits CC1_PD and CC2_PD set to 0. For the CH32X315MCU6 chip, PD4 and PD5 can only be configured as GPIO pull-down, with bits CC1_PD and CC2_PD set to 0.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		5	20	32	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		0.8*V_{DD}		V_{DD}	V
V_{HSEL}(1)	OSC_IN input pin low level voltage		0		0.2*V_{DD}	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%
I_L	XI input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

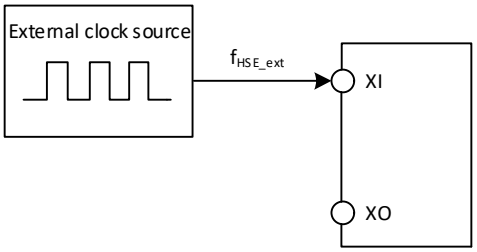


Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		5	20	32	MHz
R_F	Feedback resistance			250		kΩ
C	Recommended load capacitance and corresponding crystal series impedance R_S	R_S=60Ω(1)		20		pF
I_2	HSE drive current			0.53		mA
g_m	Oscillator transconductance	Startup		17		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} stable, 20M crystal		1(2)		ms

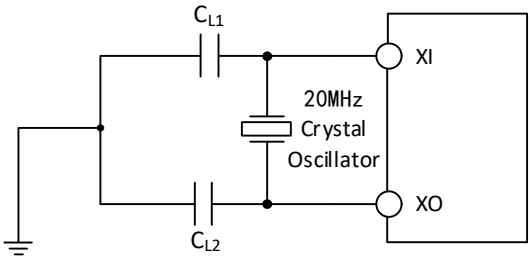
Note 1: It is recommended that the crystal's ESR does not exceed 80Ω. Prioritize crystals with lower ESR values. Refer to the crystal manual for load capacitance requirements.

2. Start time refers to the time difference from HSEON being activated until HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1}=C_{L2}.

Figure 3-5 Typical circuit of external 20M crystal



3.3.6 Internal Clock Source Characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			20		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	T_A = 0℃~70℃	-1.5		1.8	%
		T_A = -40℃~85℃	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			2	12	us
$I_{DD(HSI)}$	HSI oscillator power consumption		180	230	280	uA

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	40	60	kHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time(1)			230		us
$I_{DD(LSI)}$	LSI oscillator power consumption			1		uA

Note: 1. Set bit 1 of the RCC_RSTSCKR LSION register and wait for LSIRDY to be set to 1.

3.3.7 Wakeup Time from Low-power Mode

Table 3-13 Wakeup time from low-power mode

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	0.48	us
t_{wustop}	Wakeup from Stop mode (LDO is in normal mode)	Wake up using HSI RC clock	6.6	us
	Wakeup from Stop mode (LDO is in low-power mode)	LDO wake-up time from low power mode + HSI RC clock wake-up time	22.05	us

3.3.8 Memory Characteristics

Table 3-14 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) programming time	T_A = -40℃~85℃		1.5		ms
t_{erase_sec}	Sector erase time	T_A = -40℃~85℃		3		ms
t_{erase_block}	Block erase time	T_A = -40℃~85℃		3		ms

Note: The operating frequency of flash includes reading, programming, and erasing, and the clock comes from HCLK.

Table 3-15 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase times	T_A = 25℃	50K			Times
t_{RET}	Data retention period		20			Years

3.3.9 I/O Port Characteristics

Table 3-16 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.45*V_{DD}+0.41		V_{DD}	V
		V_{DD} = 3.3V	1.9		3.3	V
	Standard I/O pin, input high level voltage		0.45*V_{DD}+0.41		5.0	V
		V_{DD} = 3.3V	1.9		5.0	V
V_{IL}	Standard I/O pin, input low level voltage		0		0.29*V_{DD}-0.07	V
		V_{DD} = 3.3V	0		0.9	V
	Standard I/O pin, input low level voltage		0		0.29*V_{DD}-0.07	V
		V_{DD} = 3.3V	0		0.9	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis			240		mV
	FT I/O pin Schmitt trigger voltage hysteresis			220		
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Pull-up equivalent resistance		30	40	55	kΩ
R_{PD}	Pull-down equivalent resistance		30	40	55	kΩ
C_{IO}	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output) pins can handle input or output currents of up to ±8mA, and can handle input or output currents of ±20mA (without strictly adhering to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, pin sinks current	I_{IO} = 8mA		0.4	V
V_{OH}	Output high level, pin source current	2.8V < V_{DD} < 3.6V	V_{DD}-0.4		
V_{OL}	Output low level, pin sinks current	I_{IO} = 20mA		1.0	V
V_{OH}	Output high level, pin source current	2.8V < V_{DD} < 3.6V	V_{DD}-1.0		

Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 3-18 Input/Output AC characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
00	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD} = 2.8-3.6V		30	MHz
			CL=30pF, V_{DD} = 2.8-3.6V		35	MHz
			CL=10pF, V_{DD} = 2.8-3.6V		43	MHz
	$t_r/t_{f(IO)out}$	Output the rising time from low to high level, and the falling time from high to low level.	CL=50pF, V_{DD} = 2.8-3.6V		10	ns
			CL=30pF, V_{DD} = 2.8-3.6V		7.6	ns
			CL=10pF, V_{DD} = 2.8-3.6V		5	ns
01	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD} = 2.8-3.6V		32	MHz
			CL=30pF, V_{DD} = 2.8-3.6V		45	MHz
			CL=10pF, V_{DD} = 2.8-3.6V		90	MHz
	$t_r/t_{f(IO)out}$	Output the rising time from low to high level, and the falling time from high to low level.	CL=50pF, V_{DD} = 2.8-3.6V		8	ns
			CL=30pF, V_{DD} = 2.8-3.6V		5.5	ns
			CL=10pF, V_{DD} = 2.8-3.6V		3	ns
10	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD} = 2.8-3.6V		35	MHz
			CL=30pF, V_{DD} = 2.8-3.6V		50	MHz
			CL=10pF, V_{DD} = 2.8-3.6V		100	MHz
	$t_r/t_{f(IO)out}$	Output the rising time from low to high level, and the falling time from high to low level.	CL=50pF, V_{DD} = 2.8-3.6V		8	ns
			CL=30pF, V_{DD} = 2.8-3.6V		5.5	ns
			CL=10pF, V_{DD} = 2.8-3.6V		3	ns
11	$F_{max(IO)out}$	Maximum frequency	CL=50pF, V_{DD} = 2.8-3.6V		37	MHz
			CL=30pF, V_{DD} = 2.8-3.6V		55	MHz
			CL=10pF, V_{DD} = 2.8-3.6V		110	MHz

	$t_r/t_{f(IO)out}$	Output the rising time from low to high level, and the falling time from high to low level.	CL=50pF, V_{DD} = 2.8-3.6V		8	ns
			CL=30pF, V_{DD} = 2.8-3.6V		5.5	ns
			CL=10pF, V_{DD} = 2.8-3.6V		2.5	ns

Note: 1. The above are guaranteed design parameters.

3.3.10 NRST Pin Characteristics

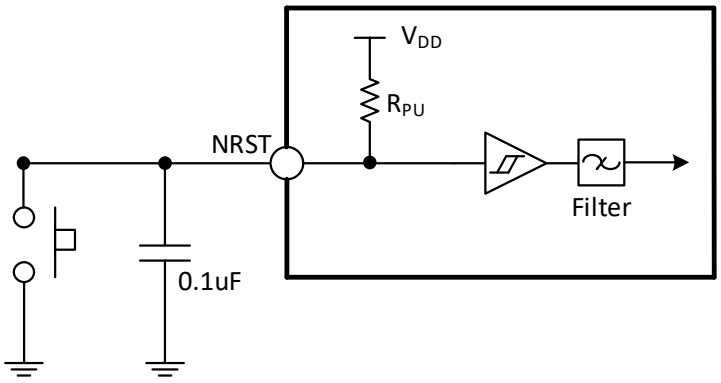
Table 3-19 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		0		0.29*V_{DD}-0.07	V
$V_{IH\ (NRST)}$	NRST input high-level voltage		0.45*V_{DD}+0.41		V_{DD}	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis			240		mV
R_{PU}(1)	Pull-up equivalent resistance		30	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse width				100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse width		300			ns

Note: The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS switch is very small (approximately 10%).

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin



Note: The capacitor shown in the diagram is optional and can be used to filter out key bounce.

3.3.11 TIM Timer Characteristics

Table 3-20-1 TIM1/2/3 characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 200MHz	5		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 200MHz	0	100	MHz
R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 200MHz	0.005	328	us
t_{MAX_COUNT}	Maximum possible count			65536	$t_{TIMxCLK}$

		$f_{TIMxCLK}$ = 200MHz		21.5	s

Table 3-20-2 TIM4 characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 200MHz	5		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 200MHz	0	100	MHz
R_{esTIM}	Timer resolution			32	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 200MHz	0.005	$2^{32}/200$	us
t_{MAX_COUNT}	Maximum possible count			2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 200MHz		$2^{32}*2^{16}/200$	us

3.3.12 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram

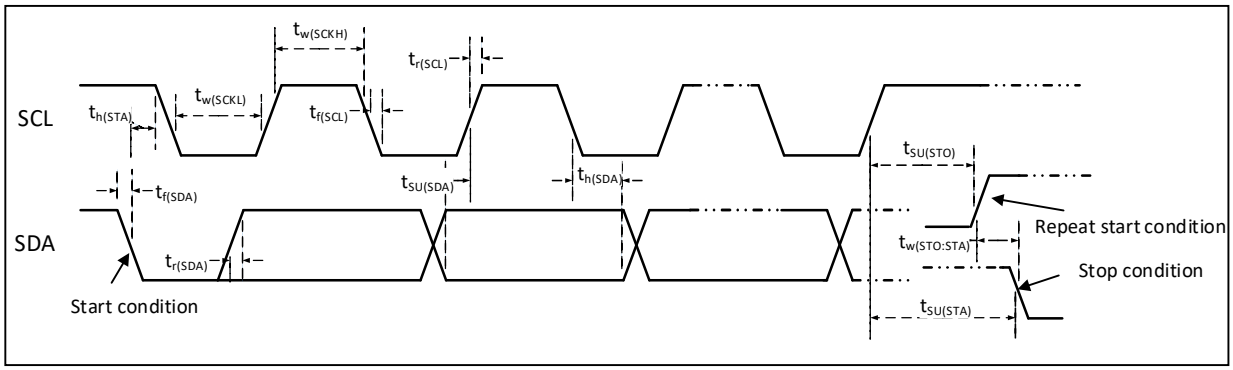


Table 3-21 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode

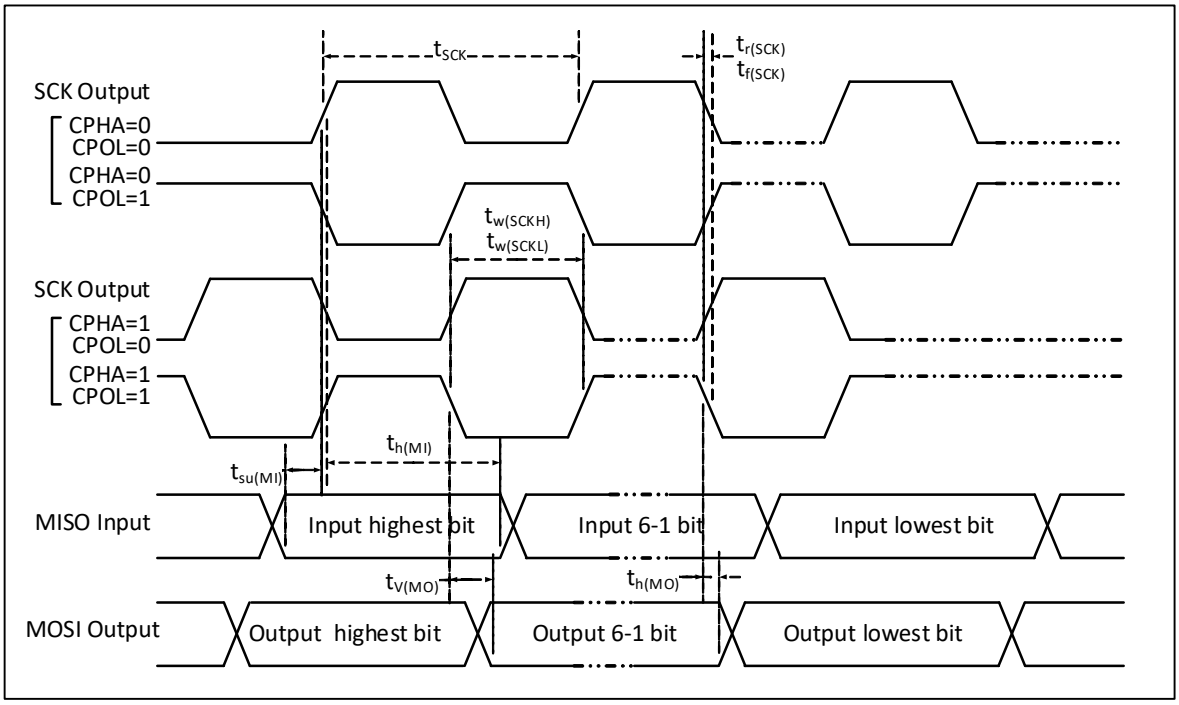


Figure 3-10 SPI timing diagram in Slave mode (CPHA=0)

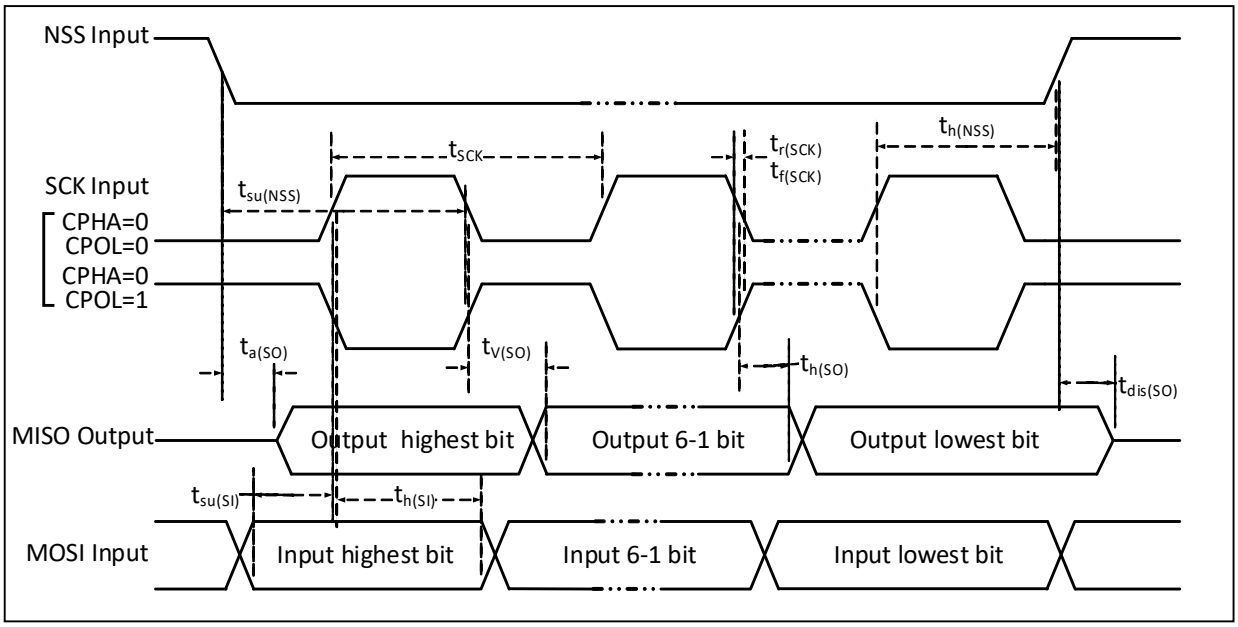


Figure 3-11 SPI timing diagram in Slave mode (CPHA=1)

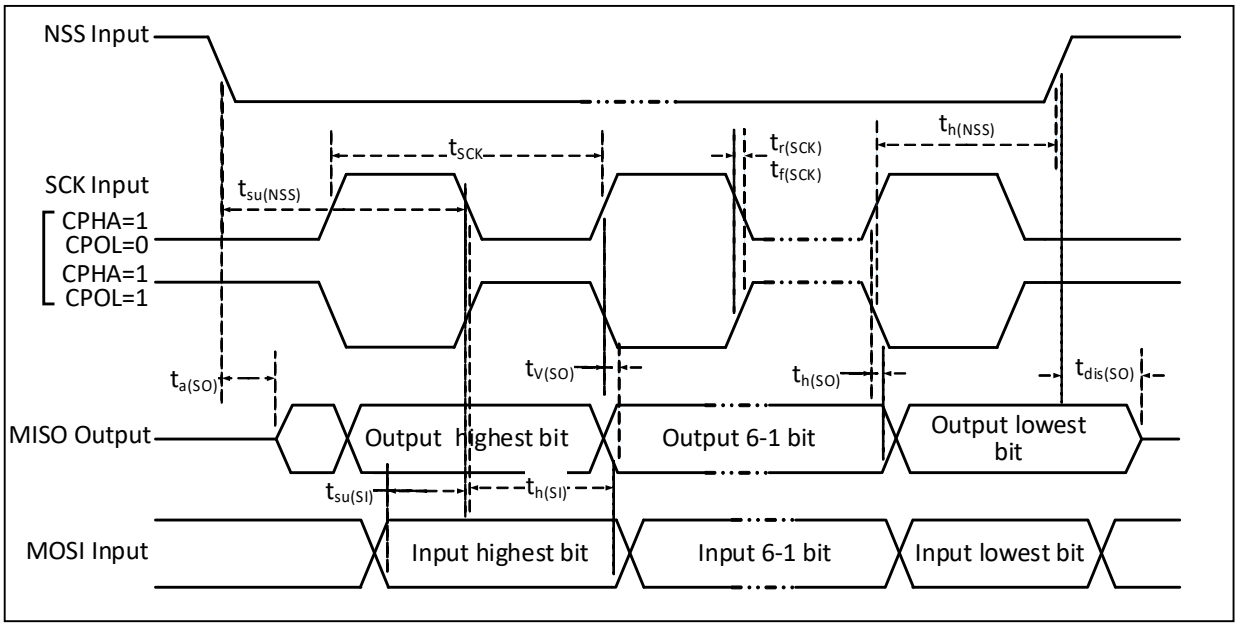


Table 3-22 SPI interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode			100	MHz
		Slave mode			100	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF			8	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode		$2*t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode		$2*t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 24MHz, Prescaler factor = 4		70	97	ns
$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	9		ns
			HSRXEN = 1	$9-0.5*t_{SCK}$		
$t_{SU(SI)}$		Slave mode		4		ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4		ns
			HSRXEN = 1	$0.5*t_{SCK}-4$		
$t_{h(SI)}$		Slave mode		4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	$1*t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	9	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			9	ns
$t_{V(MO)}$		Master mode (After enable edge)			5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)		8		ns
$t_{h(MO)}$		Master mode (After enable edge)		0		ns

3.3.14 USB PD Interface Characteristics

Table 3-23-1 PD interface I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{Rise}	Rise time	Time between 10% and 90% of amplitude,	300	400		ns

		the minimum value is the time under no load condition				
t_{Fall}	Fall time	Time between 10% and 90% of amplitude, the minimum value is the time under no load condition	300	400		ns
V_{Swing}	Output voltage swing (peak-to-peak)		1.04	1.12	1.20	V

Table 3-23-2 Type-C I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CCIL}(1)	CC pin inputs low level voltage	HVT = 0, FT I/O input	0		0.8	V
		HVT = 1, high threshold detection input	0		2.0	
V_{CCIH}(1)	CC pin input high level voltage	HVT = 0, FT I/O input	2.0		V_{DD}	V
		HVT = 1, high threshold detection input	2.45		V_{DD}	
V_{CChys}	Hysteresis voltage	HVT = 0, FT I/O input		220		mV
		HVT = 1, high threshold detection input		120		
I_{pu}	Pull-up current	PAD < V_{DD}-0.6V		80		uA
				180		uA
				330		uA
Rd	Built-in Rd pull-down resistor for CC pin (applicable to CC1R/CC2R)	V_{DD} ≥ 1.6V or external pull-up330uA	4.3	5.1	6.1	kΩ

Note 1: When HVT=1, the corresponding V_{CCIL} and V_{CCIH} are guaranteed design parameters.

3.3.15 USB2.0 Interface Characteristics

Table 3-24 USB2.0 module characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	USB2.0 operating voltage		3.15		3.45	V
V_{SE}	Single ended receiver threshold	V_{DD33} = 3.3V	1.2		1.9	V
V_{OL}	Static output low level				0.3	V
V_{OH}	Static output high level		2.8		3.6	V
V_{HSSQ}	Detection threshold of high-speed pressing information		100		150	mV
V_{HSDSC}	Detection threshold of high-speed disconnection		500		625	mV
V_{HSOI}	High-speed idle level		-10		10	mV
V_{HSOH}	High-speed data high level		360		440	mV
V_{HSOL}	High-speed data low level		-10		10	mV
R_{USBPU}	USB pin pull-up resistor		1.3	1.5	1.8	kΩ

R_{USBPD}	USB pin pull-down resistor		13	15	18	kΩ
V_{BC_REF}	BC CMP reference voltage			0.4		V
V_{BC_SRC}	BC protocol output voltage			0.6		V

3.3.16 USB3.2 Gen1 Interface Characteristics

The CH32X315 chip complies with the USB3.2 Gen1 specification. For more information, please refer to the relevant protocol specifications.

3.3.17 12-bit ADC Characteristics

Table 3-25 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.8		3.6	V
V_{REF+}(2)	Positive reference voltage	$V_{REF+} \leq V_{DDA}$	2.4	3.3	3.6	V
V_{REF-}(2)	Negative reference voltage		0	0	1.0	V
I_{DDA}	ADC supply current (excluding buffer)			1.42		mA
I_{BUF}	ADC buffer self current			0.76		mA
f_{ADC}	ADC clock frequency			16	80	MHz
f_S	Sampling rate		0.06		5	MHz
f_{TRIG}	External trigger frequency				4.4	MHz
					18	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		V_{REF-}		V_{REF+}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1.5	kΩ
C_{ADC}	Internal sample and hold capacitor			4.5		pF
t_{CAL}	Calibration time	f_{ADC} = 16MHz			31.875	us
t_{Iat}	Injection trigger conversion delay	f_{ADC} = 80MHz			0.025	us
					2	$1/f_{ADC}$
t_{Iatr}	Normal trigger conversion delay	f_{ADC} = 80MHz			0.025	us
					2	$1/f_{ADC}$
t_s	Sampling time	f_{ADC} = 80MHz	0.037		3.031	us
			3.5		242.5	$1/f_{ADC}$
t_{STAB}	Power on time	f_{ADC} = 16MHz			1	us
t_{CONV}	Total conversion time (including sampling time)		0.2		3.188	us
			16		255	$1/f_{ADC}$

Note: 1. All above are design parameters.

2. V_{REF+} and V_{REF-} external capacitors should be as close as possible, otherwise the ADC performance will be affected.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above Formula 1 is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 3-26 Maximum R_{AIN} when f_{ADC} = 80MHz

T_S(cycle)	t_S(ns)	Maximum R_{AIN}(kΩ)
3.5	43.75	0.4
5.5	68.75	1.0
7.5	93.75	1.5
13.5	168.75	3.3
20.5	256.25	5.3
30.5	381.25	8.1
45.5	568.75	12.4
68.5	856.25	19.0

Table 3-27 ADC error (f_{ADC} = 80MHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ET	Overall error	R_{AIN} < 1kΩ, V_{DDA} = 3.3V		±3.5		LSB
ED	Differential nonlinearity error			±3		
EL	Integral nonlinearity error			±4		

Note: All above are design parameters.

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-23 ADC typical connection diagram

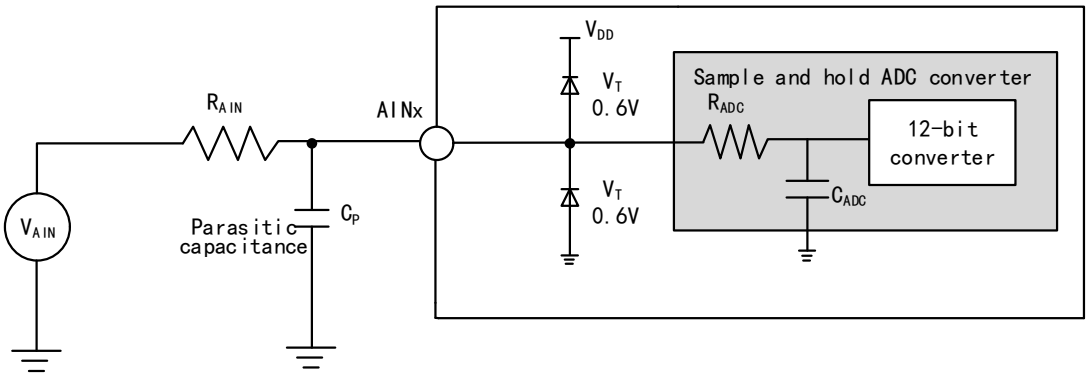
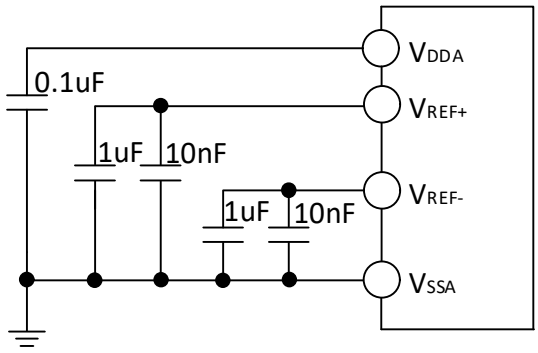


Figure 3-24 Analog power supply and decoupling circuit reference



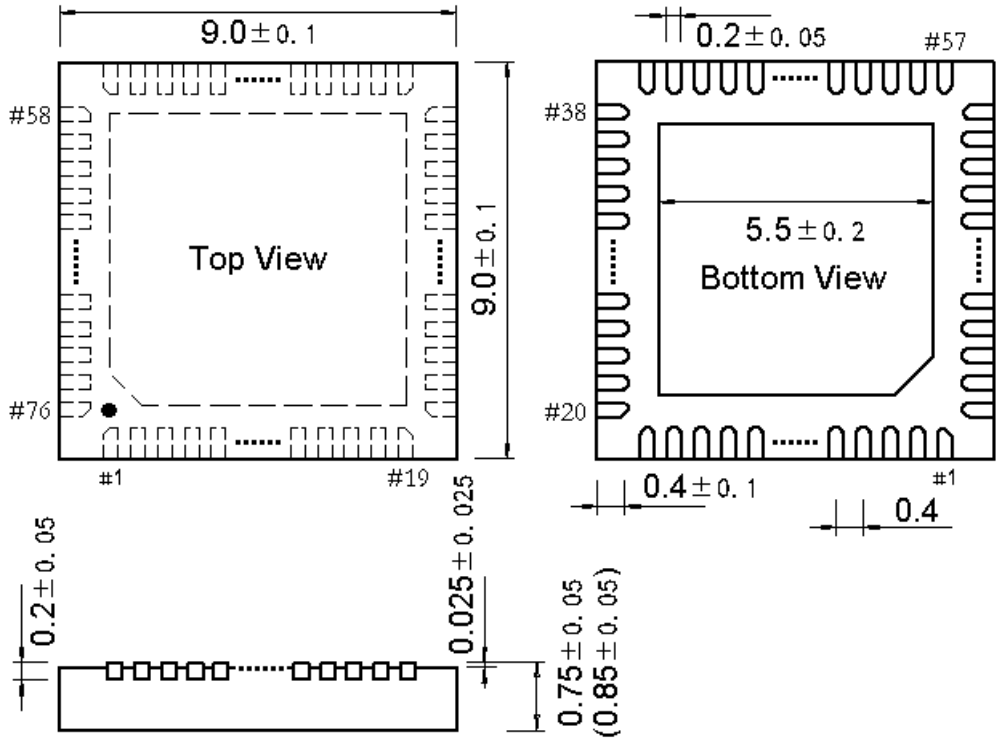
Chapter 4 Package and Ordering Information

Packages

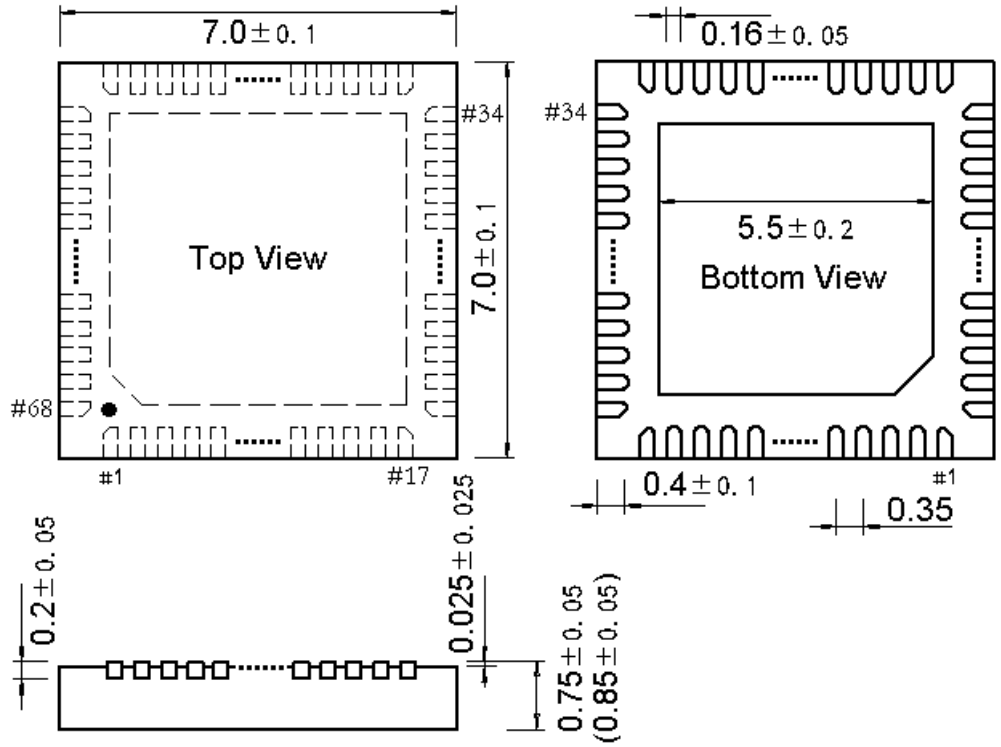
Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32X315MCU6
QFN68X7	7*7mm	0.35mm	13.8mil	Quad Flat No-lead Package	CH32X315WCU6
QFN48	5*5mm	0.35mm	13.8mil	Quad Flat No-lead Package	CH32X315CCU6
LQFP64	7*7mm	0.4mm	15.7mil	Low Profile Quad Flat Pack	CH32X305RCT6

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or ±10%.

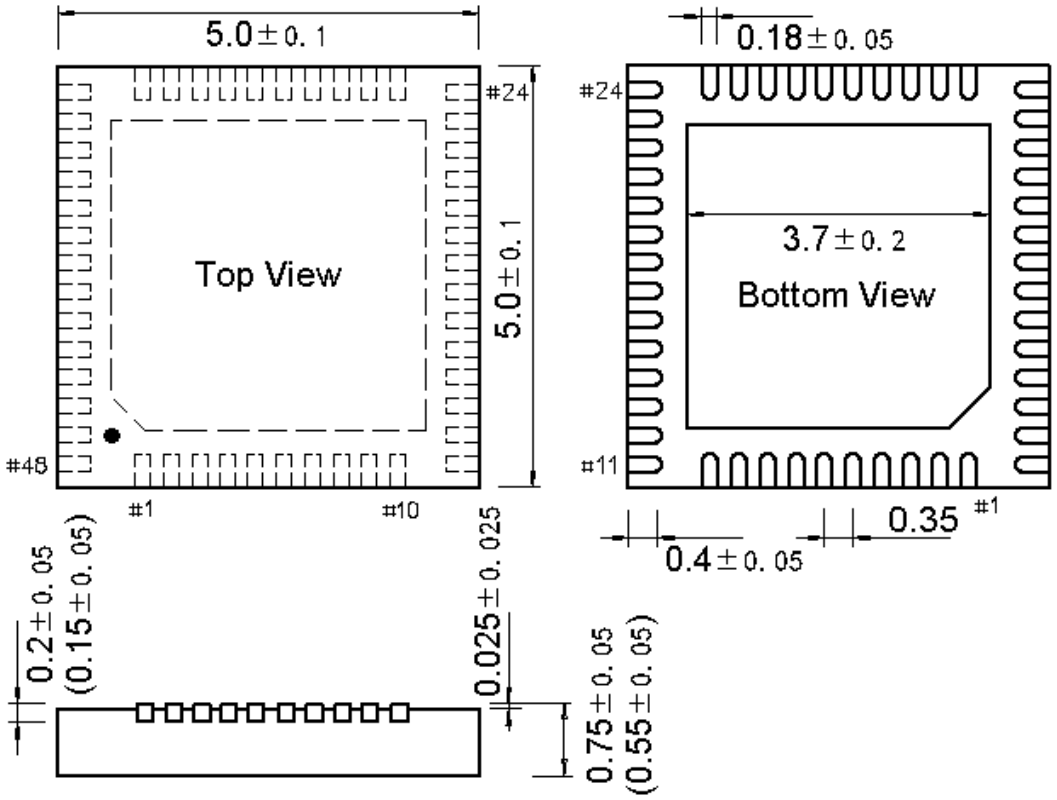
4.1 QFN76 Package



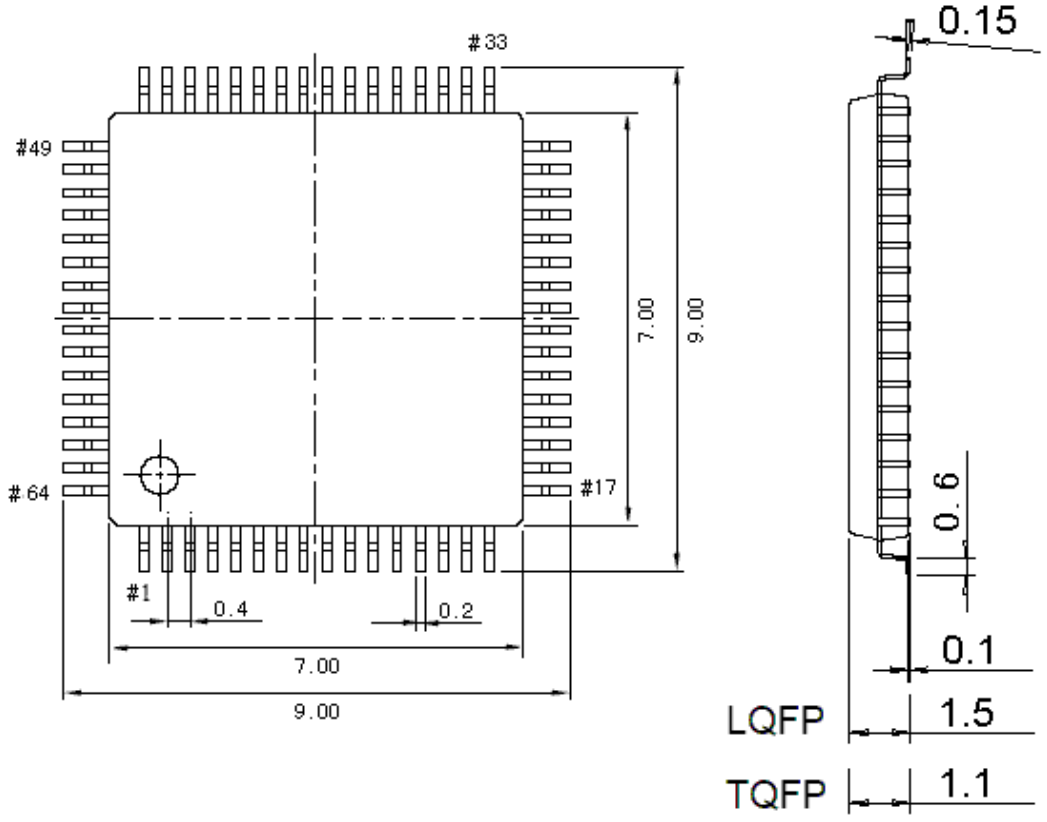
4.2 QFN68X7 Package



4.3 QFN48 Package



4.4 LQFP64 Package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Product Series

F = Arm core, general-purpose MCU
V = QingKe RISC-V core, general-purpose MCU
L = QingKe RISC-V core, low-power MCU
X = QingKe RISC-V core, dedicated or special peripheral MCU
M = QingKe RISC-V core, Built-in gate drive motor MCU
H = QingKe RISC-V core, high-performance MCU

Product type (*)+Product sub-series (**)

Product type	Product sub-series
0 = Value version, main frequency <=48M	06 = 64K Flash multi-function general-purpose type, OPA, dual-purpose, TKey 07 = Basic motor application type, OPA+CMP
1 = Basic version, main frequency <=100M 2 = Enhanced version, main frequency <=200M 3 = Hardware floating point, medium and large capacity <512KB	05 = Connected, USB HS, ADC 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 15 = Connected, USBSS, USBHS, ADC 17 = Interconnected, USB HS, CAN, Ethernet (Built-in PHY), SDIO
4 = Large capacity >=512KB	07 = Interconnected, USB HS, Ethernet (Built-in PHY), ARGB 17 = Interconnected, USB SS, SerDes, HSADC, UHSIF, SDIO, DVP, Ethernet (Built-in PHY) 67 = Interconnected, USB HS, Ethernet (Built-in PHY), ARGB、PSRAM

Pin number

J = 8 pin D = 12 pin A = 16 pin F = 20 pin E = 24 pin
G = 28 pin K = 32 pin T = 36 pin C = 48 pin R = 64 pin
W = 68 pin M = 88 pin V = 100 pin Q = 128 pin Z = 144 pin

Flash memory capacity

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory 8 = 64K Flash memory
B = 128K Flash memory C = 256K Flash memory E = 512K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40℃~85℃
7 = -40℃~105℃
3 = -40℃~125℃
D = -40℃~150℃