



Overview

CH32V407 is an industrial-grade interconnected microcontroller based on the QingKe RISC-V core. It supports zero-wait operation at a 200MHz clock speed and the V-vector instruction set, making it suitable for applications such as accelerated computing and parallel processing. The CH32V407 integrates 2 sets of USB2.0 high-speed PHY transceivers (480Mbps), an Ethernet MAC controller, and 10/100Mbps physical layer transceivers; It features integrated analog resources such as dual ADCs, dual DACs, and OPAs; it also provides a wealth of peripheral resources, including 2 sets of DMA controllers (totaling 24 channels), SDIO, DVP interfaces, RNG, ARGB, LTDC, FSMC, multiple timer units, 10 USARTs, I2C interfaces, I3Cs, 3 SPIs, 2 I2Ss, and CAN interfaces.

The CH32V467 adds 4MB or 8MB of on-chip extended PSRAM memory to the CH32V407 and supports DMA.

Features

- **Core:**
 - QingKe 32-bit RISC-V3V core, multiple instruction set combinations
 - Support V-vector instruction set, support parallel computing
 - Fast programmable interrupt controller + hardware interrupt stack
 - 2-level hardware interrupt stack
 - System main frequency up to 200MHz
- **Memory:**
 - 200KB zero-wait volatile data storage area SRAM
 - 992KB program memory CodeFlash (Zero-wait application area+Non-zero-wait data area)
 - 28KB BootLoader
 - 128B user-defined memory
- **8MB extended PSRAM memory (CH32V467 only)**
 - DMA block read/block write speed can reach 600Mbytes/s
- **Power management and low-power consumption:**
 - System power supply VDD voltage range: 2.9~3.6V
 - Low-power mode: Sleep, Stop, Standby
 - VBAT independently powers RTC and backup register
- **System clock & Reset**
 - Built-in factory-trimmed 20MHz RC oscillator
 - Built-in 40kHz RC oscillator
 - High-speed external 5~32MHz oscillator
 - Low-speed external 32.768kHz oscillator
 - Power on/down reset, programmable voltage detector
- **Real-time clock (RTC): 32-bit independent timer**
- **2 sets of 12-bit DAC**
- **2 sets of 12-bit ADC**
 - Analog input range: VSSA~VDDA
 - 16 external signals + 2 internal signals
 - Dual ADC conversion mode
- **OPA/PGA/CMP**
 - 2 input channels and 2 output channels
- **24-channel universal DMA controller (2 groups)**
- **10 sets of USART: support LIN**

- **I2C interface (Support SMBus/PMBus)**
- **I3C interface**
- **3 sets of SPI interfaces (SPI2 and SPI3 are used for I2S2 and I2S3)**
- **2 sets of 480Mbps high-speed USB2.0 controllers and PHY:**
 - Support high-speed and full-speed Host and Device modes
 - Support 1024-byte packets
- **CAN interface (2.0B active)**
- **SDIO interface (MMC, SD/SDIO cards, and CE-ATA)**
- **Flexible Static Memory Controller (FSMC)**
- **150MHz Digital Video Port (DVP)**
- **LCD-TFT Display Controller (LTDC)**
- **Random Number Generator (RNG)**
- **Addressable RGB (ARGB)**
- **100M Ethernet MAC and 10/100M PHY**
 - Fully integrated MAC and PHY; only requires external capacitors
 - Support Auto-MDIX and auto-polarity

- detection
 - 10M/100Mbps auto-negotiation; support full-duplex and half-duplex modes
- **Multiple timers**
 - 2×16-bit advanced-control timers, with dead-time control and emergency brake; can offer PWM complementary output for motor control
 - 4×16-bit general-purpose timers, providing input capture, output compare, PWM, pulse counting, and incremental encoder input
 - 2 basic timers
 - 2 watchdog timers (independent watchdog and window watchdog)
 - SysTick: 32-bit counter
- **Fast GPIO port**
 - 77 I/O ports, mapping 16 external interrupts
- **Security features: CRC calculation unit, 96-bit chip unique ID**
- **Debug mode: 1-wire (default)/2-wire serial debug interface (SDI)**
- **Package: LQFP, QFN**

Model Resource difference		CH32V407			CH32V467		
		VET6	WEU6	RET6	VET6	WEU6	RET6
Chip pin number		100	68	64	100	68	64
Zero-wait Flash (Bytes) ⁽²⁾		512K	512K	512K	512K	512K	512K
Zero-wait SRAM (Bytes) ⁽²⁾		200K	200K	200K	200K	200K	200K
Extended PSRAM (Bytes)		-	-	-	8M	8M	4M
GPIO port number		77	55	49	76	54	48
Timer	Advanced-control (16-bit) ⁽¹⁾	2	2	2	2	2	2
	General-purpose (16-bit) ⁽¹⁾	4	4	4	4	4	4
	Basic (16-bit)	2	2	2	2	2	2
	Watchdog	2 (WWDG + IWDG)			2 (WWDG + IWDG)		
	SysTick (32-bit)	Support			Support		
RTC		Support			Support		
ADC	Unit	2	2	2	2	2	2
	channel	16+2	16+2	16+2	16+2	16+2	16+2
DAC (Unit)		2	2	2	2	2	2
OPA		1	1	1	1	1	1
RNG		1	1	1	1	1	1
USART		10	10	10	10	10	10
SPI/I2S		3/2	3/2	3/2	3/2	3/2	3/2
I2C		1	1	1	1	1	1
I3C		1	1	1	1	1	1
CAN		1	1	1	1	1	1
SDIO		1	1	1	1	1	1
USBHS (Include PHY)		2	2	1 (USBHS1)	2	2	1 (USBHS1)
Ethernet		MAC+10M/100M PHY			MAC+10M/100M PHY		
DVP		1	1	1	1	1	1
FSMC		1	-	-	1	-	-
LTDC		1	1	1	1	1	1
ARGB		1	1	1	1	1	1
CPU main frequency		Max: 200MHz			Max: 200MHz		
Operating temperature		Industrial-grade: -40°C~85°C			Industrial-grade: -40°C~85°C		
Package form		LQFP100	QFN68	LQFP64	LQFP100	QFN68	LQFP64

Note: 1. Functions in the timer that involve pin signals, such as PWM and interrupt capture, must be used in conjunction with the actual pin configuration of the chip package; if certain pins are not exposed in a particular package, these functions cannot be used.

2. The 64KB of zero-wait SRAM can also be configured for use as zero-wait flash memory, resulting in 576KB of zero-wait flash memory and 136KB of zero-wait data.

Chapter 1 Specification Information

1.1 System Architecture

The microcontroller is based on the RISC-V instruction set architecture (ISA) in which the core, arbitration unit, DMA module, SRAM storage and other parts are interacted through multiple sets of buses. A general-purpose DMA controller is integrated in the chip to reduce the burden on the CPU and improve access efficiency. The application of a multi-level clock management mechanism reduces the operating power consumption of peripherals. At the same time, it has a data protection mechanism and measures such as automatic clock switching protection to increase system stability. The following figure is a block diagram of the overall internal structure of the series of products.

Figure 1-1-1 CH32V407 System block diagram

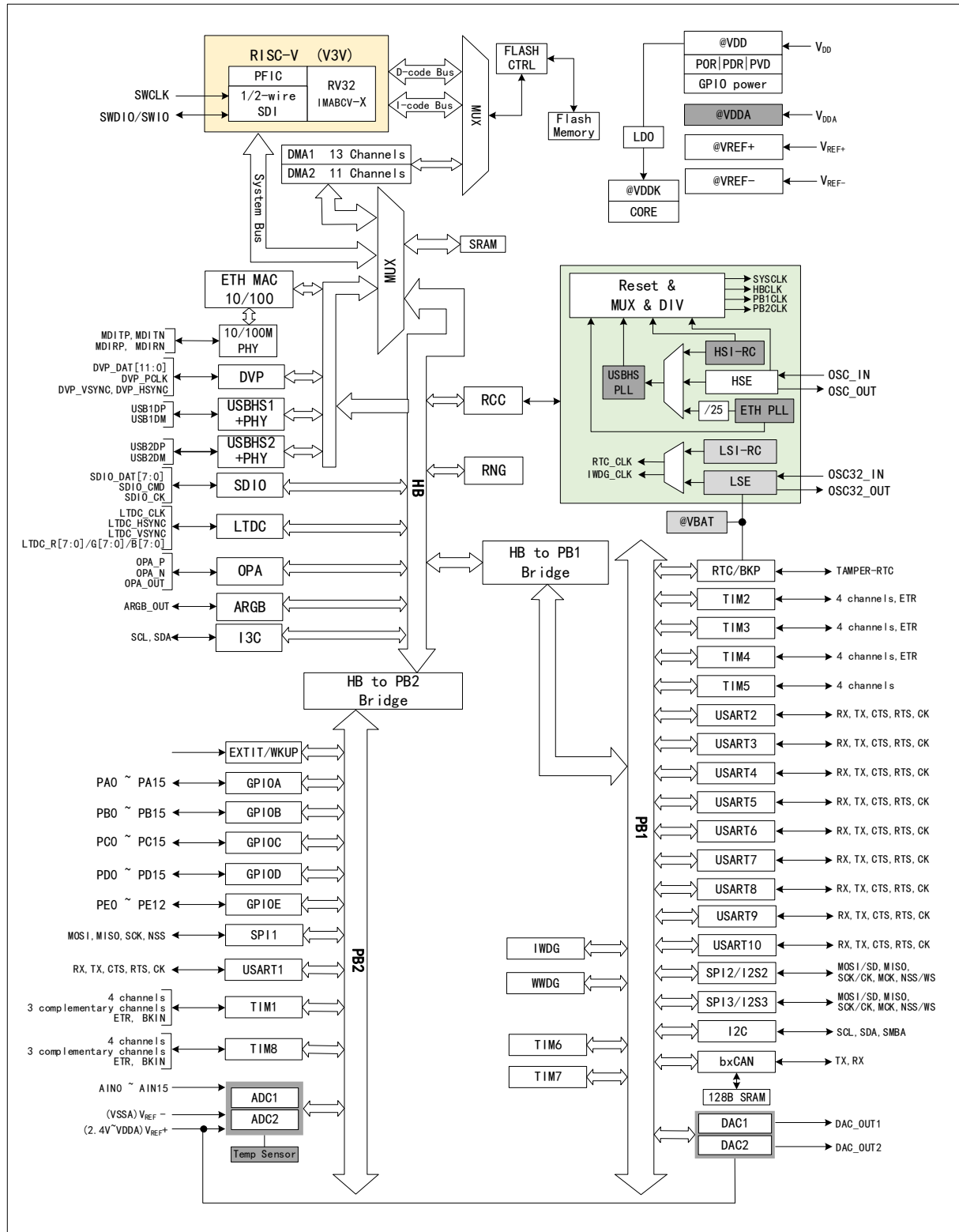


Figure 1-1-2 CH32V467 System block diagram

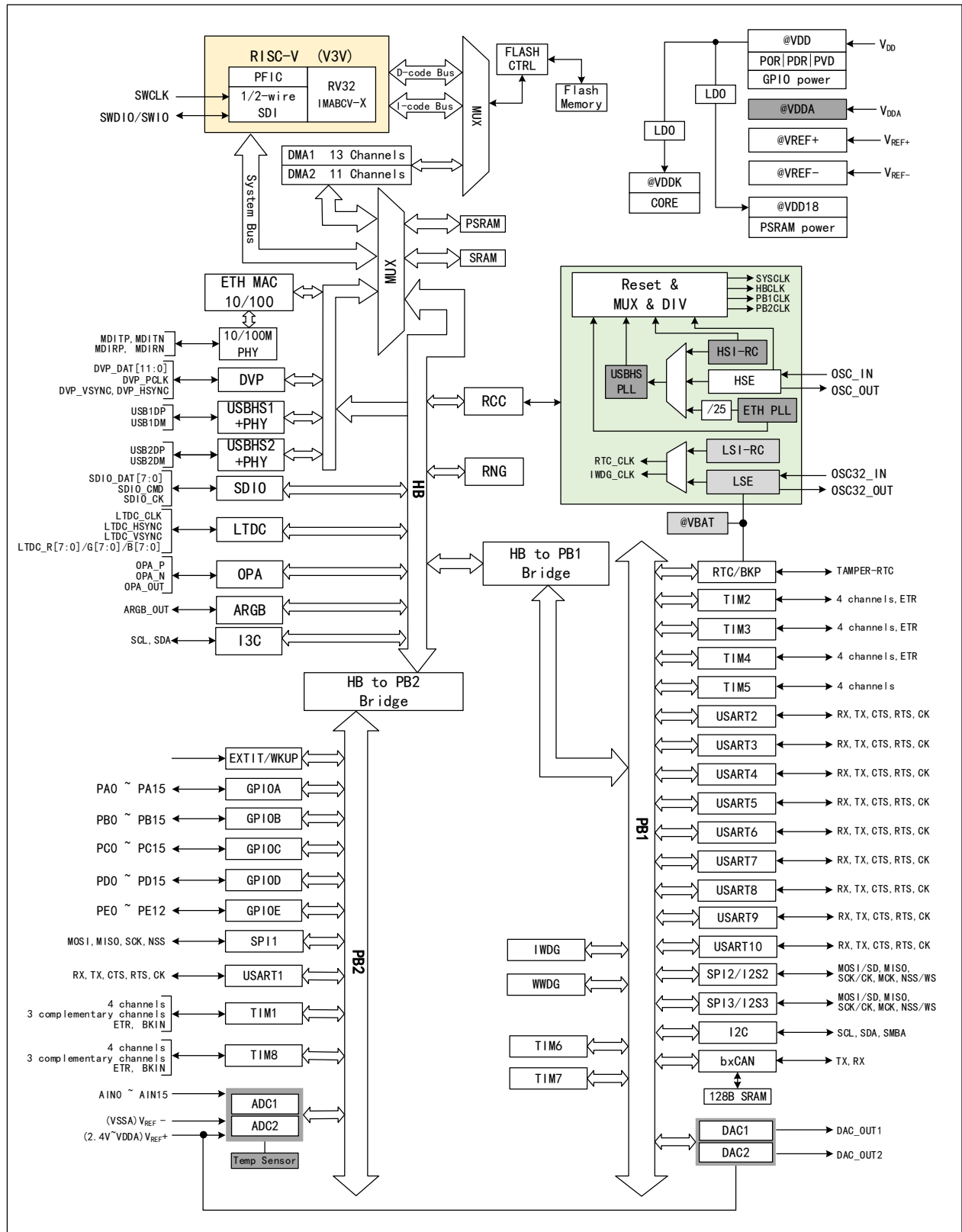
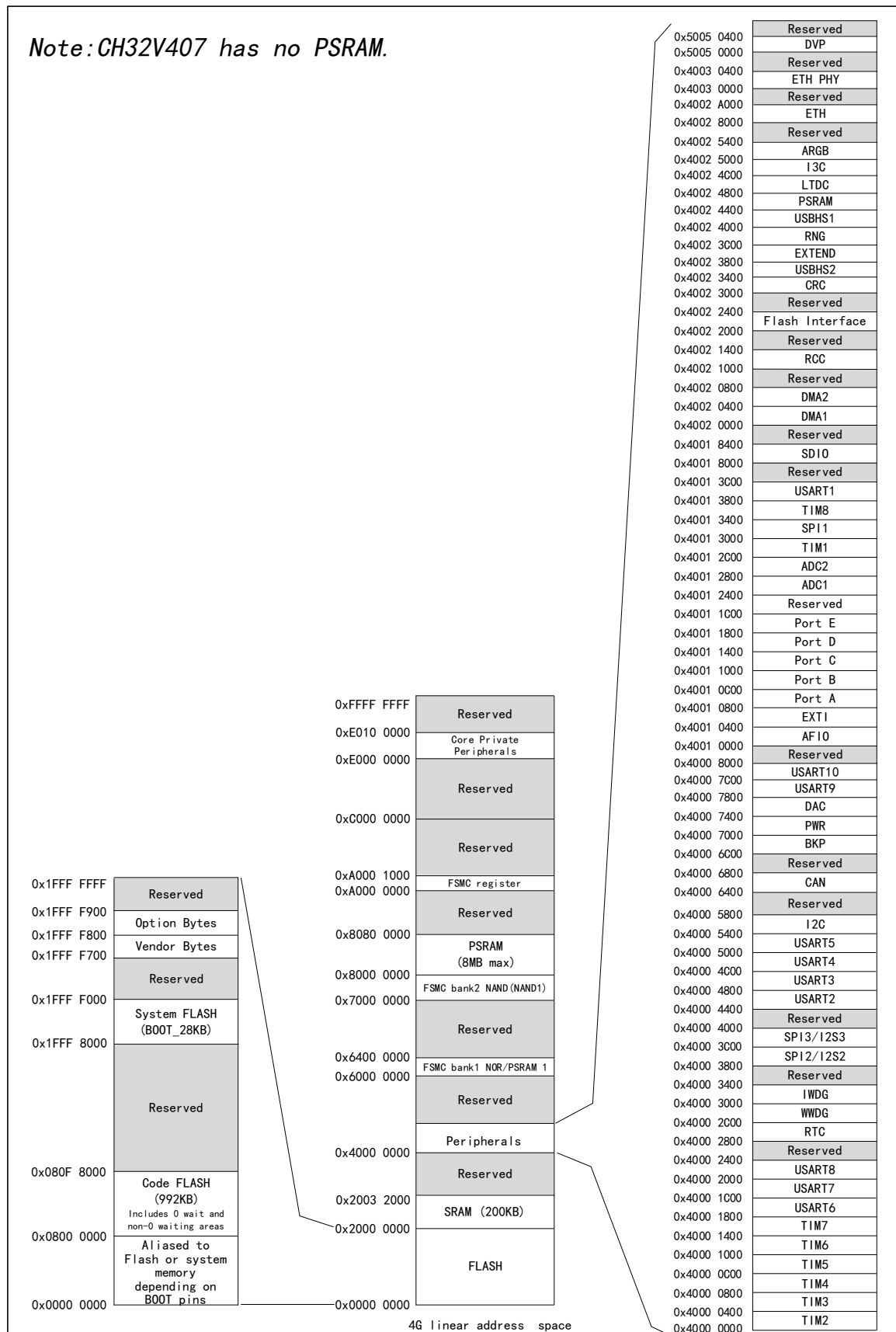


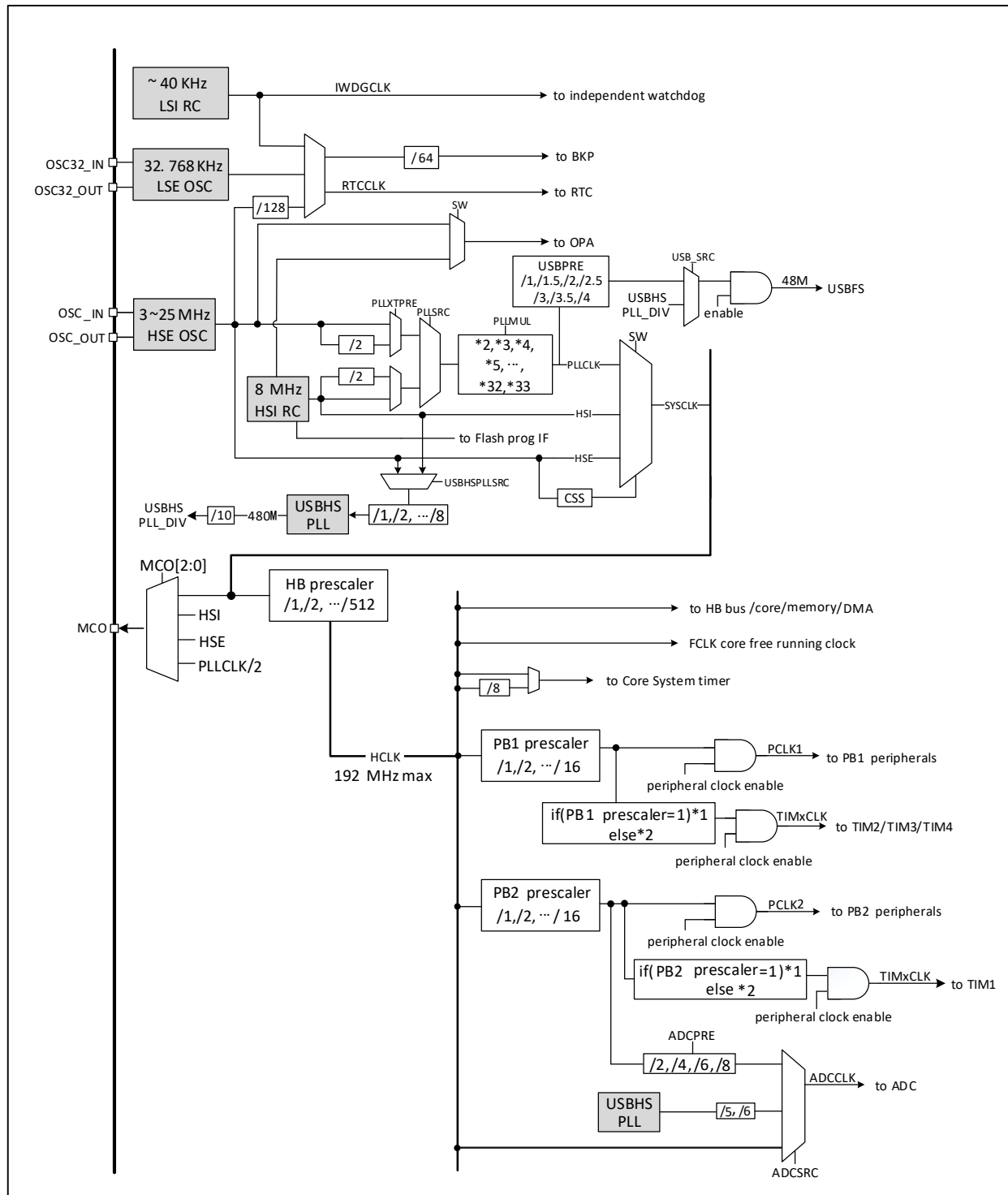
Figure 1-2 Memory address map



1.3 Clock Tree

4 groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE).

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V3V Processor

RISC-V3V supports the ICBM-X subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as fast programmable interrupt controller (PFIC) and extended instruction support. Externally multiple buses are connected to external unit modules to enable interaction between external function modules and the core.

The processor can be flexibly applied in different scenarios, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc., due to its minimal instruction set, multiple working modes, and modular customization extensions.

- Sequential single-issue architecture
- 2–3-stage pipeline
- Provide a non-maskable interrupt (NMI)
- 2-level interrupt nesting
- Fast Programmable Interrupt Controller (PFIC)
- Support bit operation instructions
- Support custom extended instructions
- Hardware interrupt stack
- Vector operation/parallel processing

1.4.2 On-chip Memory and Boot Mode

Built-in zero-wait 200K byte SRAM area is used to store data, which will be lost after power failure.

Built-in 992K bytes program flash memory storage area (Code FLASH), i.e. user area, for user's application program and constant data storage. This includes a 480K byte non-zero-wait program area and a 512K byte zero-wait program execution area.

64KB of the zero-wait data SRAM can be configured for zero-wait programs, resulting in a 416KB non-zero-wait program area, a 576KB zero-wait program execution area, and a 136 KB zero-wait data SRAM area.

Built-in 28 bytes System FLASH (System FLASH), i.e. BOOT area, used for system boot program storage, built-in bootstrap loading program.

Built-in 128 bytes system non-volatile configuration information storage area, used for vendor's configuration word storage, factory-cured, user cannot be modified.

Built-in 128 bytes user-defined information storage area for user option byte storage.

At startup, one of three bootstrap modes can be selected via the bootstrap pins (BOOT0 and BOOT1):

- Bootstrap from program flash memory
- Boot from system memory
- Boot from internal SRAM

The bootstrap loading program is stored in the system memory and the contents of the program flash memory storage area can be reprogrammed via the USART1 and USB interfaces.

Note: For chips w with the fifth last digit of the lot number is greater than 0, their non-zero waiting area

supports two 64-bit accesses, RVV instruction and DMA.

1.4.3 On-chip Extended PSRAM Memory

On the basis of CH32V407, CH32V467 chip also has built-in extended PSRAM memory of 4M or 8M bytes, which supports data storage through address and reading and writing instructions and DMA. Its main features include:

- 8-bit hardware width, supporting 8-bit, 16-bit, or 32-bit random or block reads and writes
- Support clock rates up to 300MHz, supports both rising and falling edges, and supports data transfer rates up to 600Mbps
- Support write data masking
- Support high-speed read operations via data gating
- Support register-configurable write and read initial delays
- Support semi-sleep mode and deep sleep mode

1.4.4 Power Supply Scheme

(1) CH32V407

- $V_{DD} = 2.9\sim 3.6V$: It supplies power to the I/O pins and the system voltage regulator (LDO), including power to the integrated USB PHY and Ethernet PHY. At the same time, V_{DD} supplies power to the integrated system voltage regulator (LDO) and outputs a regulated power supply on the V_{DDK} pin. The V_{DD} pin adjacent to the Ethernet signal pins is the main V_{DD} pin; it is recommended to connect a 0.1uF high-frequency capacitor in parallel with at least 4.7uF of capacitance. For the other V_{DD} pins, it is recommended to connect a 0.1uF high-frequency capacitor. When used for USB 2.0 or Ethernet, the recommended V_{DD} range is 3.15 to 3.45V. When the chip enters stop mode (LDO configured as low power mode) or enters standby mode, V_{DD} cannot be lower than 3.0V.
- $V_{DDA} = 2.9\sim 3.6V$: Supplies power to the analog portion of the high-frequency RC oscillator, ADC, OPA, DAC and PLL. It is recommended to externally connect a high frequency capacitor with a capacity of 0.1uF.
- $V_{REF+} = 2.4\sim 3.6V$: For the positive reference voltage used by the ADC, it is recommended to connect an external high-frequency capacitor with a capacitance of 0.1uF. The V_{REF+} voltage must not exceed the V_{DDA} voltage.
- V_{REF-} : Negative reference voltage for the ADC; it is recommended to connect this pin to V_{SS} .
- $V_{DDK} = 1.17\sim 1.27 V$: Supplies power to the core circuitry; it is recommended to connect a 0.1uF capacitor in parallel with a 2.2uF high-frequency capacitor. During normal operation, the V_{DDK} voltage is generated by the system voltage regulator (LDO) powered by V_{DD} . To reduce the heat generated by the chip's internal LDO, this power supply may be sourced externally (e.g., from an external DC-DC converter); the recommended external supply voltage should be slightly higher than the internal LDO output voltage.
- $V_{BAT} = 1.8\sim 3.6V$: Optional backup power supply. When V_{DD} and V_{DDA} is turned off, the internal power switch switches to V_{BAT} to provide power exclusively to the RTC and external low-frequency oscillator.

The power pins with the same names above must be shorted. The voltage relationship is: $V_{DD} = V_{DDA}$; and $V_{DDA} \geq V_{REF+}$.

(2) CH32V467

- $V_{DD} = 2.9\sim 3.6V$: Power supply for I/O pin, system voltage regulator LDO and on-chip PSRAM voltage regulator LDO_1.8V, including power supply for built-in USB PHY and Ethernet PHY. At the same time, V_{DD} supplies power to the built-in LDO and LDO_1.8V, and outputs regulated power on V_{DDK} and

V_{DD18} pins respectively. The V_{DD} pin adjacent to the Ethernet signal pins is the main V_{DD} . It is recommended to connect a 0.1uF high-frequency capacitor in parallel with at least 10uF of high-frequency capacitance, and the total capacitance should not be less than the combined total capacitance of V_{DDK} and V_{DD18} . For other V_{DD} pins, it is recommended to connect a 0.1uF high-frequency capacitor. When used for USB2.0 or Ethernet, the recommended V_{DD} range is 3.15 to 3.45 V.

- $V_{DDA} = 2.9\sim 3.6V$: Supplies power to the analog portion of the high-frequency RC oscillator, ADC, OPA, DAC and PLL. It is recommended to externally connect a high frequency capacitor with a capacity of 0.1uF.
 - $V_{DD18} = 1.2\sim 2$ V: Supplies power to the on-chip PSRAM module. It is recommended to connect a high-frequency capacitor with a total capacitance of 0.1uF in parallel with 2.2uF. During normal operation, the V_{DD18} voltage is generated by the V_{DD} -powered PSRAM voltage regulator LDO_1.8V and can be disabled via software.
 - $V_{REF+} = 2.4\sim 3.6V$: For the positive reference voltage used by the ADC, it is recommended to connect an external high-frequency capacitor with a capacitance of 0.1uF. The V_{REF+} voltage must not exceed the V_{DDA} voltage.
 - V_{REF-} : Negative reference voltage for the ADC; it is recommended to connect this pin to V_{SS} .
 - $V_{DDK} = 1.17\sim 1.27$ V: Supplies power to the core circuitry; it is recommended to connect a 0.1uF capacitor in parallel with a 2.2uF high-frequency capacitor. During normal operation, the V_{DDK} voltage is generated by the system voltage regulator (LDO) powered by V_{DD} . To reduce the heat generated by the chip's internal LDO, this power supply may be sourced externally (e.g., from an external DC-DC converter); the recommended external supply voltage should be slightly higher than the internal LDO output voltage.
 - $V_{BAT} = 1.8\sim 3.6V$: Optional backup power supply. When V_{DD} and V_{DDA} is turned off, the internal power switch switches to V_{BAT} to provide power exclusively to the RTC and external low-frequency oscillator.
- The power pins with the same names above must be shorted. The voltage relationship is: $V_{DD} = V_{DDA}$; and $V_{DDA} \geq V_{REF+}$.

1.4.5 Power Supply Detector

The chip integrates a power-on reset (POR)/power-off reset (PDR) circuit, which is always in a working state; when V_{DD} falls below the set threshold ($V_{POR/PDR}$), it puts the device in reset without the need for an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage magnitude of the V_{DD} supply with the set threshold V_{PVD} . Turning on the corresponding edge interrupt of the PVD allows you to receive an interrupt notification when V_{DD} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for $V_{POR/PDR}$ and V_{PVD} values.

1.4.6 System Voltage Regulator LDO

After resetting, the system voltage regulator LDO is automatically switched on. There are 3 modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.
- Shutdown mode: The regulator is automatically switched to this mode when the CPU enters the Standby mode, the regulator output is high resistance, the power supply to the core circuit is cut off, and the

regulator is in the zero-consumption state.

The regulator is always in on mode after reset, and is turned off in standby mode in shutdown mode, when it is high resistance output.

1.4.7 Low-power Mode

The system supports 3 low-power modes, which can achieve the best balance under the conditions of low-power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

This mode FLASH enters the low-power mode or power-off state, and the RC oscillator and HSE crystal oscillator of PLL and HSI are turned off. The stop mode can achieve the lowest power consumption while keeping the contents of SRAM and registers intact.

Exit condition: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 77 external I/O ports, PVD output, RTC alarm clock, I3C wake-up signal or USB wake-up signal.

- Standby mode (STANDBY)

In this mode, the main LDO of the system is turned off, the wake-up circuit is powered by the low-power LDO, all other digital circuits are powered off, and the FLASH is in a power-off state. The wake-up system from standby mode will reset and SBF (PWR_CSR) will be set. After waking up, the SBF status is queried to know the low-power mode before wake-up, and the SBF is cleared by the CSBF (PWR_CR) bit. In standby mode, the contents of 32KB's SRAM can be maintained (depending on the planned configuration before going to bed), and the contents of the backup register can be retained.

Exit conditions: Any external event (EXTI signal), external reset signal on NRST, IWDG reset, rising edge on WKUP, in which EXTI signal includes one of 77 external I/O ports, RTC alarm clock, etc.

1.4.8 Programmable Fast Interrupt controller (PFIC)

The product has a built-in Programmable Fast Interrupt Controller (PFIC), which supports up to 256 interrupt vectors, and provides flexible interrupt management functions with minimal interrupt latency. The current product manages 7 core private interrupts and 88 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in user and machine privileged modes.

- Support hardware interrupt stack (HPE) without instruction overhead
- Vector table free interrupts (VTF) response mechanism, 4 programmable direct interrupt vector addresses
- Vector table supports address or command mode
- Configurable interrupt nesting depth, up to 2 levels

1.4.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 22 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both

edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal PB2. Up to 77 general-purpose I/O ports can be connected to 16 external interrupt lines.

1.4.10 General DMA Controller

The system has built-in 2 groups of general-purpose DMA controllers, manages 24 channels in total, including 13 channels in DMA1 and 11 channels in DMA2. Flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general/advanced/basic TIMx, ADC, DAC, I2S, USART, I2C, SPI, SDIO, ARGB.

Note: DMA1, DMA2 and CPU access the system SRAM after arbitration by the arbiter.

1.4.11 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 5~32MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of HB. The high-speed PB (PB2) and low-speed PB (PB1) regions provide peripheral clocks with a maximum frequency of 200MHz. Refer to the clock tree block diagram in Figure 1-3.

Ethernet or high-speed USB applications do not support HSI, so external crystal HSE is usually needed.

1.4.12 Real Time Clock (RTC) and Backup Registers

The RTC and the backup register are in the backup power supply area inside the system. When V_{DD} is valid, it is powered by V_{DD} , and when V_{DD} is invalid, the internal power is automatically switched to the V_{BAT} pin.

RTC is a set of 32-bit programmable counters, and its time base supports 20-bit prescaler, which is used for long-time measurement. The clock reference comes from high-speed external clock (HSE/128) 128 frequency division, external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the setting and time of RTC can remain unchanged after the system is reset or awakened from standby mode.

The backup register contains up to 42×16 -bit registers, which can be used to store 84 bytes of user application data. This data can continue to be maintained after wake-up from Standby, or system Reset or power Reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

1.4.13 Analog-to-digital Converter (ADC)

The chip has built-in 2×12 -bit ADC that provides up to 16 external channels and 2 internal channel samples

with programmable channel sampling times for single, continuous, sweep or intermittent conversion. Provides analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages, provides configurable analog watchdog reset function to reset the system when monitored voltage exceeds a threshold. Supports external event-triggered transitions. Trigger sources include internal signals from on-chip timers and external pins. Supports operation using DMA.

ADC internal channel sampling includes one channel sampling with built-in temperature sensor and one channel sampling with internal reference power supply. The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel for converting the output of the sensor into a digital value.

1.4.14 Digital-to-Analog Converter (DAC)

The chip integrates 2×12-bit voltage-output digital-to-analog converters (DACs) that convert two digital signals into two analog voltage signals for output. It supports independent or synchronous conversion of the dual DAC channels, 12-bit data left-aligned or right-aligned, 12-bit or 8-bit data, and external event-triggered conversion. It can generate triangular waves and noise. It supports DMA functionality.

1.4.15 Timer and Watchdog

The timers in the system include advanced-control timers, general-purpose timers, basic timers, watchdog timers, and system clock timers. The number of timers included varies across different products in the series; please refer to Table 1-1 for details.

Table 1-1 Timer comparison

Timer		Resolution ratio	Counting type	Time base	DMA	Function
Advanced-control timer	TIM1	16-bit	Upcount	PB2 time domain	Support	PWM complementary output, single pulse output
	TIM8		Downcount Up/downcount	16-bit frequency divider		Input capture Output compare Timing counting
General-purpose timer	TIM2	16-bit	Upcount Downcount Up/downcount	PB1 time domain 16-bit frequency divider	Support	Input capture Output compare Timing counting
	TIM3					
	TIM4					
	TIM5					
Basic timer	TIM6	16-bit	Upcount	PB1 time domain 16-bit frequency divider	Support	Timing counting
	TIM7					
Window watchdog		7-bit	Downcount	PB1 time domain 4 kinds of frequency division	Not support	Timing Reset system (normal operation)
Independent watchdog		12-bit	Downcount	PB1 time	Not	Timing

			domain 7 kinds of frequency division	support	Reset system (Normal+low power operation)
System time base timer	32-bit	Up/downcount	HCLK or HCLK/8	Not support	Timing

- Advanced-control timer

The advanced-control timer is two 16-bit automatic load increment/decrement counter(TIM1 and TIM8) with 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a 3-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer

The general-purpose timer is four 16-bit (TIM2, TIM3, TIM4 and TIM5) autoloader counters with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation, and single pulse mode output. It can also work with advanced control timers through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen while PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Any general timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process the signal of the incremental encoder and the digital output of 1 to 3 Hall sensors.

- Basic timer

The basic timer module includes two 16-bit auto-reset timers (TIM6 and TIM7) used for counting and generating interrupts or DMA requests upon event completion. The basic timers support 16-bit programmable prescalers and can provide a clock signal to a digital-to-analog converter (DAC) or trigger the DAC's synchronization circuit. The basic timers are independent of one another and do not share any resources.

- Independent watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 40KHz. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window watchdog (WWDG)

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- System time base timer (SysTick)

QingKe microprocessor core comes with a 32-bit optional increment or decrement counter, which is used to generate SYSTICK exceptions (exception number: 12), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, or can be used as a standard 32-bit counter. It has

automatic reload function and programmable clock source.

1.4.16 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 10 sets of Universal Synchronous/Asynchronous Transceivers (USART1/2/3/4/5/6/7/8/9/10). Full-duplex asynchronous communication, synchronous unidirectional communication, and half duplex single line communication are supported, as well as LIN (Local Interconnect Network), ISO7816 compatible smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation for continuous communication.

1.4.17 Serial Peripheral Interface (SPI)

Up to 3 groups of serial peripherals interface provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

1.4.18 I2S (Audio) Interface

Up to 2 standard I2S interfaces (shared with SPI2 and SPI3) operate in master or slave mode. They are software-configurable for 16-bit or 32-bit data packet transmission frames, support audio sampling rates ranging from 8 kHz to 562.2kHz, and support four audio standards. In master mode, its master clock can be output to an external DAC or CODEC (decoder) at a fixed frequency of 256 times the audio sampling rate, and supports DMA.

1.4.19 I2C Bus

The chip features a built-in I2C bus interface capable of operating in either master or slave mode, and supports all I2C-specific timing, protocols, and arbitration. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0/PMBus bus.

1.4.20 I3C Bus

The I3C bus is a 2-wire serial single-ended multi-branch bus designed to improve the traditional I2C bus. The I3C interface is responsible for handling communication between the device and other devices connected to the I3C bus. It itself supports both as a master and a slave, and when used as a controller, it can enhance the functionality of the I2C interface while maintaining a certain degree of backward compatibility. The main features include:

- Support master/slave device
- Support MIPI I3C specification v1.1
- Support DMA
- Support In-Band Interrupt (IBI) function
- Hot join (HJ) function
- Built-in error detection and recovery
- I3C SCL bus clocking up to 12.5MHz
- Support dynamically assigned addresses, direct and broadcast Common Command Code (CCC), and

private read/write transfers

1.4.21 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbps/s, and it supports time-triggered communication functions. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and two 3-level deep receiving FIFOs.

Products with a single CAN controller have only 14 configurable filters and feature a dedicated 128-byte SRAM for sending and receiving data.

1.4.22 Universal Serial Bus USB2.0 High-speed Host/Device Controller (USBHS)

The USB2.0 High-Speed Controller serves dual roles as both a host controller and a device controller. When functioning as a host controller, it supports USB devices operating at low-speed, full-speed, and high-speed modes; when functioning as a device controller, it can be flexibly configured to operate in low-speed, full-speed, or high-speed modes to accommodate various applications. The chip integrates 2 sets of USB2.0 high-speed host/device controllers and two sets of 480Mbps USB PHY transceivers, forming two independent USB systems. The main features include:

- Support USB 2.1, USB 2.0, USB 1.1, and USB 1.0 protocol specifications
- Support data rates of 480 Mbps, 12 Mbps, and 1.5 Mbps
- Feature 2 built-in high-speed PHYs and 2 controllers, supporting both USB Host and USB Device modes
- Support control transfers, bulk transfers, interrupt transfers, and real-time/synchronous transfers
- Provide bus reset, suspend, wake-up, and resume functions
- Host supports USB HUB
- All non-zero endpoints support up to 1024-byte packets with built-in FIFO, supporting interrupts and DMA

1.4.23 Digital Video Port (DVP)

DVP (Digital Video Port) is used to connect the camera module to obtain image data stream. It provides 8/10/12-bit parallel interface communication, and supports up to 150MHz pixel clock input frequency. It supports image data organized in the original row and frame format, such as YUV, RGB, etc., and also supports compressed image data such as JPEG format, which can receive high-speed parallel data streams output by external 8-bit, 10-bit, and 12-bit camera modules. During reception, it mainly relies on VSYNC and HSYNC signal synchronization. Supports image cropping function.

1.4.24 SDIO Controller

The SDIO interface provides the operation interface of multimedia card (MMC), SD memory card, SDIO card and CE-ATA device. Supports 3 different data bus modes: 1-bit (default), 4-bit and 8-bit. The SDIO clock frequency is selectable; during actual data transmission, it supports either 4-wire mode (up to 80MHz) or 8-wire mode (up to 50MHz). Currently, this interface is fully compatible with multimedia card system specification 4.2 (forward compatible), SDIO card specification 3.0, SD I/O card specification 2.0, SD memory card specification 3.0 UHS-I, and CE-ATA digital protocol specification 1.1. The main features include:

- Support SD card, SDIO card and MMC/eMMC card

- Support master or slave mode
- Support 1-bit, 4-bit and 8-bit bus modes
- Support read/write data blocks in any byte unit.
- SDIO supports clock frequency optional, 4-wire mode up to 80MHz, 80-wire mode up to 50MHz
- Compatible with MMC specification 4.5 (forward compatible)
- Compatible with SD card Specification 3.0, SDIO card specification 2.0
- Not compatible with SPI
- Support DMA

1.4.25 Flexible Static Memory Controller (FSMC)

The FSMC interface mainly provides synchronous or asynchronous memory interfaces and supports SRAM, PSRAM, NOR and NAND devices. The internal HB transmission signal is converted into an appropriate external communication protocol, allowing continuous access of 8/16/32 bits of data. And that sample delay time can be flexibly configured to meet the time sequence of different devices.

In addition, FSMC can also be used for most graphic LCD controller interfaces, supporting the modes of Intel 8080 and Motorola 6800, facilitating the construction of a simple graphic application environment, or for a high-performance scheme of a special acceleration controller.

1.4.26 LCD-TFT Display Controller (LTDC)

LCD-TFT (Liquid Crystal Display-Thin Film Transistor) Display Controller (LTDC) mainly provides parallel digital RGB and horizontal synchronization, vertical synchronization, pixel clock and data enabled signals, which can be used as output signals to different LCD and TFT panel interfaces. Its main characteristics are:

- Provide 1 display layers containing proprietary 8*32-bit FIFOs
- Support Color Look-Up Tables (CLUT) with up to 256 colors per layer
- Support Programmable timing of different display panels
- Support programmable background colors
- Support programmable polarity of HSYNC, VSYNC and data enable signals
- Up to 8 input color formats per display layer: ARGB8888, RGB888, RGB565, ARGB1555, ARGB4444, L8 (8-bit luminance or CLUT), AL44 (4-bit alpha + 4-bit luminance), AL88 (8-bit alpha + 8-bit luminance)
- Support programmable window position and size
- Support thin-film transistor (TFT) color displays
- Support up to 3 programmable interrupt times

1.4.27 Addressable RGB (ARGB)

The chip incorporates a set of ARGB (Addressable RGB) modules, supporting configurable high and low logic levels for 0-code and 1-code signals, as well as DMA.

The ARGB modules enable timing control for single-data-line RGB light strips and support single-wire RGB daisy-chaining. Compared to traditional RGB, they can drive a wider range of ARGB lighting control ICs, enabling a greater variety of lighting effects.

1.4.28 Ethernet Controller and Transceiver (MAC+PHY)

The chip has a built-in Gigabit Ethernet controller (MAC) that complies with IEEE802.3-2002 standards, which acts as the data link layer. Its Link speed supports up to 100Mbps with auto-negotiation. When used in

applications, it enables the development of network products in conjunction with the TCP/IP protocol stack. The chip also features a built-in 10/100Mbps Ethernet PHY, allowing for Ethernet communication using a single chip. The main features include:

- Conforms to IEEE 802.3 protocol specification and design
- Support full-duplex operation and 10/100Mbps data transmission rate
- Hardware Automatic IPv4 and IPv6 packet integrity check, IP/ICMP/UDP/TCP packet checksum calculation and auto-filling
- Multiple MAC address filtering modes
- Support 2 LED states⁽¹⁾
- Support Ethernet controller MAC + built-in 10/100Mbps PHY
- Support Auto-MDIX switching of RX/TX and automatic identification of positive and negative signal lines

Note: 1. For chips with bit ETH_LED_EN = 0 in register FEATURE_SIGN, LED0 and LED1 only provide LINK function.

1.4.29 Random Number Generator (RNG)

The chip has a built-in hardware random number generator, based on continuous analog noise, which provides a 32-bit random number through internal analog circuitry.

1.4.30 Operational Amplifier (OPA/PGA)

The chip integrates one operational amplifier (OPA or PGA) and can also function as a voltage comparator; both its input and output can be configured to select from multiple channels. It features built-in PGA gain adjustment resistors, supporting multiple amplification levels such as 4, 8, 16, and 32. It supports amplifying external analog small signals for input to an ADC to enable small-signal ADC conversion, and can also function as a signal comparator, with the comparison results output via GPIO or directly connected to the input channel of TIMx.

1.4.31 General-purpose Input and Output (GPIO)

The system provides 5 groups of GPIO ports (PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE12) with a total of 80 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port.

Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the IO configuration to avoid accidental writing to the I/O register.

All I/O pins in the system are powered by V_{DD} , which is rated at 3.3 V. When V_{DD} is de-energized, pins PC13 ~ PC15 automatically switch to being powered by V_{BAT} .

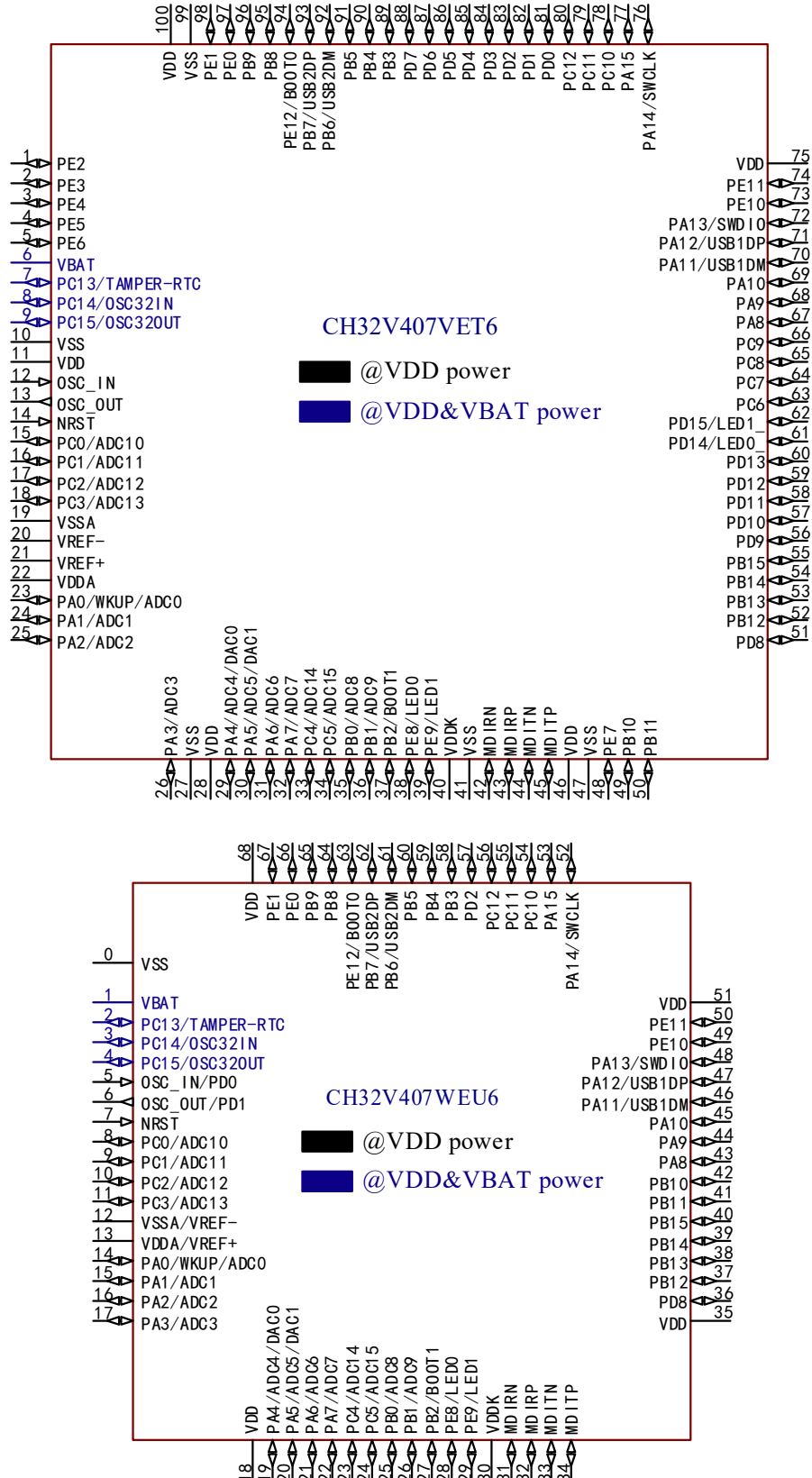
1.4.32 Serial Debug Interface (SDI)

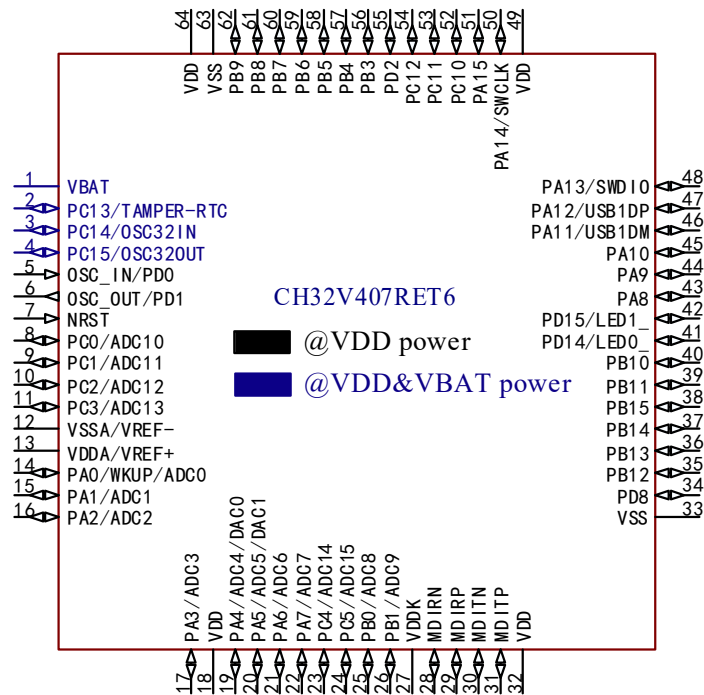
The core includes a built-in 1-wire SDI Serial Debug Interface and a 2-wire SDI Serial Debug Interface. The system supports both 1-wire and 2-wire debug modes. 1-wire debugging is the default mode, utilizing the SWIO pin (Single Wire Input Output). 2-wire debugging employs the SWDIO and SWCLK pins, enhancing download speeds during application. Upon power-up or reset, the debug interface pins default to active functionality. After the main program runs, SDI can be disabled as needed.

Chapter 2 Pinouts and Pin Definition

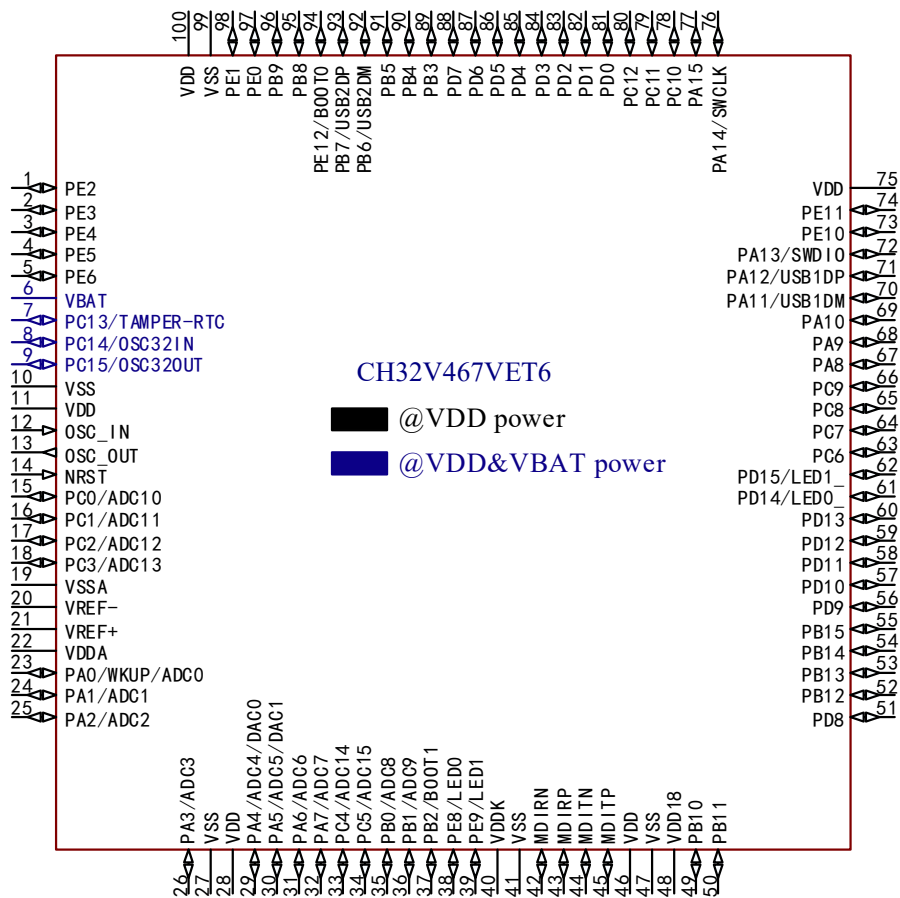
2.1 Pinout

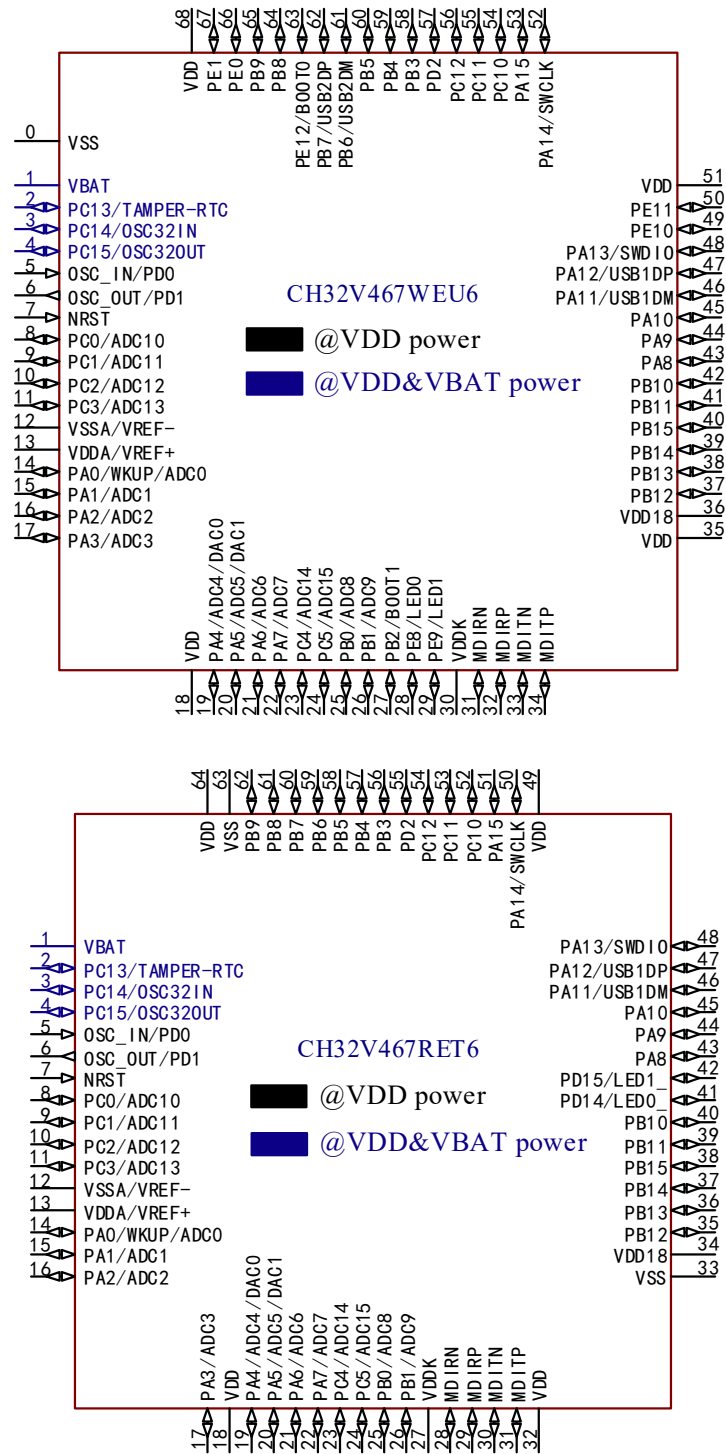
2.1.1 CH32V407 Pinouts





2.1.2 CH32V467 Pinouts





Note: Alternate functions are abbreviated in the pin diagram.

Example:

ADC_: (ADC0:ADC_IN0)

USB1DP: USBHS1_DP

USB1DM: USBHS1_DM

USB2DP: USBHS2_DP

USB2DM: USBHS2_DM

2.2 Pin Definitions

Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 2-1 CH32V407 and CH32V467 pin definitions

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
-	-	0	0	-	-	VSS	P	-	VSS		
-	-	-	-	1	1	PE2	I/O	FT	PE2	FSMC_A23	USART9_CK_2/ USART9_CK_3/ FSMC_A23_1
-	-	-	-	2	2	PE3	I/O	FT	PE3	FSMC_A19	USART9_TX_2/ USART9_TX_3/ FSMC_A19_1
-	-	-	-	3	3	PE4	I/O	FT	PE4	FSMC_A20	USART9_RX_2/ USART9_RX_3/ FSMC_A20_1
-	-	-	-	4	4	PE5	I/O	FT	PE5	FSMC_A21	USART9_CTS_2/ USART9_CTS_3/ FSMC_A21_1
-	-	-	-	5	5	PE6	I/O	FT	PE6	FSMC_A22	USART9_RTS_2/ USART9_RTS_3/ FSMC_A22_1
1	1	1	1	6	6	V _{BAT}	P	-	V _{BAT}		
2	2	2	2	7	7	PC13- TAMPER-RTC ⁽²⁾	I/O	-	PC13 ⁽³⁾	TAMPER-RTC	TIM8_CH4_1
3	3	3	3	8	8	PC14- OSC32_IN ⁽²⁾	I/O/A	-	PC14 ⁽³⁾	OSC32_IN/ USART10_CTS	USART10_CTS_1
4	4	4	4	9	9	PC15- OSC32_OUT ⁽²⁾	I/O/A	-	PC15 ⁽³⁾	OSC32_OUT/ USART10_RTS	USART10_RTS_1
-	-	-	-	10	10	V _{SS}	P	-	V _{SS}		
-	-	-	-	11	11	V _{DD}	P	-	V _{DD}		
5	5	5	5	12	12	OSC_IN	I/A	-	OSC_IN		PD0 ⁽⁴⁾
6	6	6	6	13	13	OSC_OUT	O/A	-	OSC_OUT		PD1 ⁽⁴⁾
7	7	7	7	14	14	NRST	I	-	NRST		

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
8	8	8	8	15	15	PC0	I/O/A	-	PC0	ADC_IN10/USART6_TX/LTDC_R0	USART6_TX_3/LTDC_R0_1
9	9	9	9	16	16	PC1	I/O/A	-	PC1	ADC_IN11/USART6_RX/USART7_CK/LTDC_R1	USART6_RX_3/LTDC_R1_1
10	10	10	10	17	17	PC2	I/O/A	-	PC2	ADC_IN12/USART6_CTS/USART7_TX/LTDC_R2	USART6_CTS_3/LTDC_R2_1
11	11	11	11	18	18	PC3	I/O/A	-	PC3	ADC_IN13/USART6_RTS/USART7_RX/LTDC_R3	USART6_RTS_3/LTDC_R3_1
12	12	12	12	19	19	V _{SSA}	P	-	V _{SSA}		
				20	20	V _{REF-}	P	-	V _{REF-}		
13	13	13	13	21	21	V _{REF+}	P	-	V _{REF+}		
				22	22	V _{DDA}	P	-	V _{DDA}		
14	14	14	14	23	23	PA0-WKUP	I/O/A	-	PA0	WKUP/ADC_IN0/USART2_CTS/TIM2_CH1 ⁽¹⁰⁾ /TIM2_ETR ⁽¹⁰⁾ /TIM5_CH1/TIM8_ETR	TIM2_CH1_2 ⁽¹⁰⁾ /TIM2_ETR_2 ⁽¹⁰⁾ /TIM8_ETR_1
15	15	15	15	24	24	PA1	I/O/A	-	PA1	ADC_IN1/USART2_RTS/TIM5_CH2/TIM2_CH2/LTDC_R4	TIM2_CH2_2/LTDC_R4_1
16	16	16	16	25	25	PA2	I/O/A	-	PA2	ADC_IN2/TIM2_CH3/TIM5_CH3/USART2_TX/LTDC_R5	TIM2_CH3_1/LTDC_R5_1
17	17	17	17	26	26	PA3	I/O/A	-	PA3	ADC_IN3/TIM2_CH4/TIM5_CH4/USART	TIM2_CH4_1/LTDC_R6_1

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
										T2_RX/ LTDC_R6	
-	-	-	-	27	27	V _{SS}	P	-	V _{SS}		
18	18	18	18	28	28	V _{DD}	P	-	V _{DD}		
19	19	19	19	29	29	PA4	I/O/A	HS	PA4	ADC_IN4/DAC1_OUT/ USART2_CK/SPI1_NSS/ DVP_HSYNC	USART9_TX_1/ SPI3_NSS_1/ I2S3_WS_1/ LTDC_G5_1/ DVP_HSYNC_1
20	20	20	20	30	30	PA5	I/O/A	HS	PA5	ADC_IN5/DAC2_OUT/ SPI1_SCK/DVP_VSYNC/ OPA_N2	USART1_CK_3/ USART1_CTS_2/ USART6_CK_3/ USART9_RX_1/ DVP_VSYNC_1
21	21	21	21	31	31	PA6	I/O/A	HS	PA6	ADC_IN6/TIM8_BKIN/ TIM3_CH1/SPI1_MISO/ DVP_PCLK/OPA_P2	TIM1_BKIN_1/ USART1_TX_3/ USART7_TX_1/ DVP_PCLK_1
22	22	22	22	32	32	PA7	I/O/A	HS	PA7	ADC_IN7/TIM8_CH1N/ TIM3_CH2/USART8_CK/ SPI1_MOSI/LTDC_R7/ OPA_OUT1	TIM1_CH4_3/ TIM1_CH1N_1/ USART1_RX_3/ USART7_RX_1/ LTDC_R7_1
23	23	23	23	33	33	PC4	I/O/A	-	PC4	ADC_IN14/ USART7_CTS/ USART8_TX/LTDC_G0	USART1_CTS_3/ USART4_CTS_1/ USART7_CTS_1/ FSMC_D4_1/ LTDC_G0_1
24	24	24	24	34	34	PC5	I/O/A	-	PC5	ADC_IN15/USART7_RTS/ USART8_RX/LTDC_G1	USART1_RTS_3/ USART4_RTS_1/ USART7_RTS_1/ LTDC_G1_1
25	25	25	25	35	35	PB0	I/O/A	-	PB0	ADC_IN8/TIM8_CH2N/	TIM1_CH2N_1/ TIM3_CH3_2/

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
										TIM3_CH3/USART6_CK/ USART8_CTS/LTDC_G2	USART4_TX_1/ USART5_CTS_2/ USART5_CTS_3/ USART7_CK_1/ LTDC_G2_1
26	26	26	26	36	36	PB1	I/O/A	-	PB1	ADC_IN9/TIM3_CH4/ TIM8_CH3N/OPA_OUT2/ USART8_RTS/ USART9_TX/LTDC_G3	TIM1_CH3N_1/ TIM3_CH4_2/ USART4_RX_1/ USART5_RTS_2/ USART5_RTS_3 LTDC_G3_1
-	-	27	27	37	37	PB2 ⁽⁵⁾	I/O	FT	PB2 BOOT1 ⁽⁵⁾	USART9_RX/LTDC_G4/ BOOT1	USART4_CK_1/ USART5_CK_2/ USART5_CK_3
-	-	28	28	38	38	PE8	I/O	FT	PE8	LED0/USART9_CTS/ FSMC_D5	TIM1_CH1N_3/ USART5_TX_2/ USART5_TX_3/ USART9_CTS_1/ FSMC_D5_1
-	-	29	29	39	39	PE9	I/O	FT	PE9	LED1/TIM1_CH1_3/ USART9_RTS/FSMC_D6	USART5_RX_2/ USART5_RX_3/ USART9_RTS_1/ FSMC_D6_1
27	27	30	30	40	40	V _{DDK}	P	-	V _{DDK}		
-	-	-	-	41	41	V _{SS}	P	-	V _{SS}		
28	28	31	31	42	42	MDIRN ⁽¹¹⁾	ETH	-	MDIRN		
29	29	32	32	43	43	MDIRP ⁽¹¹⁾	ETH	-	MDIRP		
30	30	33	33	44	44	MDITN ⁽¹¹⁾	ETH	-	MDITN		
31	31	34	34	45	45	MDITP ⁽¹¹⁾	ETH	-	MDITP		
32	32	35	35	46	46	V _{DD}	P	-	V _{DD}	Main V _{DD}	
33	33	-	-	47	47	V _{SS}	P	-	V _{SS}		
-	-	-	-	-	48	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR_3
34	-	36	-	48	-	V _{DD18}	P	-	V _{DD18}		
40	40	42	42	49	49	PB10	I/O	FT	PB10	USART3_TX/I3C_SCL/ LTDC_B3	TIM1_BKIN_3/ TIM2_CH3_2/ TIM2_CH3_3/ LTDC_B3_1

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
39	39	41	41	50	50	PB11	I/O	FT	PB11	USART3_RX/I3C_SDA/ FSMC_D9/LTDC_B2	TIM2_CH4_2/ TIM2_CH4_3/ USART8_CK_2/ USART8_CK_3/ LTDC_B2_1/ FSMC_D9_1
-	34	-	36	51	51	PD8	I/O	FT	PD8	USART9_CK/FSMC_D13/ LTDC_G5	USART3_TX_3/ USART9_CK_1/ FSMC_D13_1
35	35	37	37	52	52	PB12	I/O/A	FT, HS	PB12	TIM1_BKIN/OPA_P1/ USART3_CK/SPI2_NSS/ I2S2_WS/FSMC_D10/ LTDC_G6	USART8_RTS_2/ USART8_RTS_3/ LTDC_G6_1/ FSMC_D10_1
36	36	38	38	53	53	PB13	I/O/A	FT, HS	PB13	TIM1_CH1N/OPA_N1/ USART3_CTS/ SPI2_SCK/I2S2_CK/ FSMC_D11/LTDC_G7	USART3_CTS_1/ USART8_CTS_2/ USART8_CTS_3/ LTDC_G7_1/ FSMC_D11_1
37	37	39	39	54	54	PB14	I/O	FT, HS	PB14	TIM1_CH2N/ USART3_RTS/ SPI2_MISO/FSMC_D12/ SDIO_D0 ⁽⁶⁾ /LTDC_B0	USART3_RTS_1/ USART8_RX_2/ USART8_RX_3/ LTDC_B0_1/ SDIO_D0_1/ FSMC_D12_1
38	38	40	40	55	55	PB15	I/O	FT, HS	PB15	TIM1_CH3N/SPI2_MOSI/I2S2_SD/SDIO_D1 ⁽⁶⁾ /LTDC_B1	USART1_TX_2/ USART8_CK_1/ USART8_TX_2/ USART8_TX_3/ LTDC_B1_1/ SDIO_D1_1
-	-	-	-	56	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX_3/ FSMC_D14_1
-	-	-	-	57	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK_2/

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
											USART3_CK_3/ USART10_CK_2/ USART10_CK_3/ FSMC_D15_1
-	-	-	-	58	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS_2/ USART3_CTS_3/ USART10_TX_2/ USART10_TX_3/ FSMC_A16_1
-	-	-	-	59	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1_1/ USART3_RTS_2/ USART3_RTS_3/ USART10_RX_2/ USART10_RX_3/ FSMC_A17_1
-	-	-	-	60	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2_1/ USART10_CTS_2 USART10_CTS_3 FSMC_A18_1
41	41	-	-	61	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3_1/ USART10_RTS_2US ART10_RTS_3LED0 _1/ FSMC_D0_1
42	42	-	-	62	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4_1/ LED1_1/ FSMC_D1
-	-	-	-	63	63	PC6	I/O	FT	PC6	TIM8_CH1/I2S2_ MCK/ SDIO_D6	TIM3_CH1_3
-	-	-	-	64	64	PC7	I/O	FT	PC7	TIM8_CH2/I2S3_ MCK/ SDIO_D7	TIM3_CH2_3
-	-	-	-	65	65	PC8	I/O	FT	PC8	TIM8_CH3/ SDIO_D0 ⁽⁶⁾ /DVP_ D2	TIM3_CH3_3/ USART7_CTS_3
-	-	-	-	66	66	PC9	I/O	FT	PC9	TIM8_CH4/ SDIO_D1 ⁽⁶⁾ /DVP_ D3	TIM3_CH4_3/ USART7_RTS_3

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
										D3	
43	43	43	43	67	67	PA8	I/O	FT	PA8	MCO/TIM1_CH1/ USART1_CK/I2S3 _MCK/ LTDC_B4	TIM1_CH1_1/ USART1_CK_1/ USART1_RX_2/ USART7_CK_2/ USART7_CK_3/ LTDC_B4_1/ DVP_D2_1
44	44	44	44	68	68	PA9	I/O	FT	PA9	TIM1_CH2/USAR T1_TX /DVP_D0	TIM1_CH2_1/ USART1_RTS_2/ USART7_TX_2/ USART7_TX_3/ LTDC_DE_1/ SDIO_D6_1/ DVP_D0_1
45	45	45	45	69	69	PA10	I/O	FT	PA10	TIM1_CH3/USAR T1_RX/ DVP_D1	TIM1_CH3_1/ USART1_CK_2/ USART7_RX_2/ USART7_RX_3/ LTDC_CLK_1/ SDIO_D7_1/ DVP_D1_1
46	46	46	46	70	70	PA11	I/O/A	-	PA11	TIM1_CH4/USAR T1_CTS/ USBHS1_DM/CAN N_RX	TIM1_CH4_1/ USART1_CTS_1
47	47	47	47	71	71	PA12	I/O/A	-	PA12	TIM1_ETR/USAR T1_RTS/ USBHS1_DP/CAN _TX	TIM1_ETR_1/ USART1_RTS_1
48	48	48	48	72	72	PA13	I/O	FT	SWDIO	USART4_CTS/SW DIO/ SWIO/LTDC_B5	TIM8_CH1N_1/ USART3_TX_2/ USART6_CK_2/ LTDC_B5_1
-	-	49	49	73	73	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N_3/ USART6_TX_2/ USART8_CTS_1/ FSMC_D7_1

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
-	-	50	50	74	74	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2_3/ USART6_RX_2/ USART8_RTS_1/ FSMC_D8_1
49	49	51	51	75	75	V _{DD}	P	-	V _{DD}		
50	50	52	52	76	76	PA14	I/O	FT	SWCLK	SWCLK/LTDC_B6	TIM8_CH2N_1/ USART3_RX_2/ USART6_CTS_2/ USART8_TX_1/ LTDC_B6_1
51	51	53	53	77	77	PA15	I/O	FT, HS	PA15	SPI3_NSS/I2S3_WS/ LTDC_B7/ARGB_OUT	TIM8_CH3N_1/ TIM2_CH1_1 ⁽¹⁰⁾ / TIM2_ETR_1 ⁽¹⁰⁾ / TIM2_CH1_3 ⁽¹⁰⁾ / TIM2_ETR_3 ⁽¹⁰⁾ / USART6_RTS_2/ USART8_RX_1/ SPI1_NSS_1/ LTDC_B7_1
52	52	54	54	78	78	PC10	I/O	FT, HS	PC10	USART4_TX/SDIO_D2/ DVP_D8	USART3_TX_1/ SPI3_SCK_1/ I2S3_CK_1/ SDIO_D2_1/ DVP_D8_1
53	53	55	55	79	79	PC11	I/O	FT, HS	PC11	USART4_RX/SDIO_D3/ DVP_D4	USART3_RX_1/ SPI3_MISO_1/ SDIO_D3_1/ DVP_D4_1
54	54	56	56	80	80	PC12	I/O	FT, HS	PC12	USART4_CK/ USART5_TX/ SDIO_CK/DVP_D9	USART3_CK_1/ SPI3_MOSI_1/ I2S3_SD_1/ SDIO_CK_1/ DVP_D9_1
-	-	-	-	81	81	PD0 ⁽⁴⁾	I/O/A	FT	PD0	FSMC_D2	CAN_RX_3/ FSMC_D2_1
-	-	-	-	82	82	PD1 ⁽⁴⁾	I/O/A	FT	PD1	FSMC_D3	CAN_TX_3/ FSMC_D3_1
55	55	57	57	83	83	PD2	I/O	FT	PD2	TIM3_ETR/USAR	TIM3_ETR_1/

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
										T4_RTS/ USART5_RX/SDIO_CMD/ O_CMD/ FSMC_NADV/DVP_D11	TIM3_ETR_2/ SDIO_CMD_1/ DVP_D11_1/
-	-	-	-	84	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS_1/ FSMC_CLK_1
-	-	-	-	85	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS_1/ FSMC_NOE_1
-	-	-	-	86	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX_1/ FSMC_NWE_1
-	-	-	-	87	87	PD6	I/O	FT	PD6	FSMC_NWAIT/DVP_D10	USART2_RX_1/ FSMC_NWAIT_1
-	-	-	-	88	88	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK_1/ FSMC_NE1_1/ FSMC_NCE2_1
56	56	58	58	89	89	PB3	I/O	FT, HS	PB3	USART5_CTS/ SPI3_SCK/I2S3_CK/ DVP_D5 ⁽⁷⁾	TIM2_CH2_1/ TIM2_CH2_3/ USART5_CK_1/ SPI1_SCK_1/ LTDC_G4_1/ DVP_D5_1
57	57	59	59	90	90	PB4	I/O	FT, HS	PB4	USART5_RTS/ SPI3_MISO/ LTDC_HSYNC	TIM3_CH1_2/ USART5_TX_1/ I3C_SCL_1 SPI1_MISO_1/ DVP_D3_1
58	58	60	60	91	91	PB5	I/O	FT, HS	PB5	USART5_CK/ I2C_SMBA/SPI3_MOSI I2S3_SD/LTDC_VSYNC	TIM3_CH2_2/ USART5_RX_1/ USART6_CK_1/ I3C_SDA_1 SPI1_MOSI_1/ DVP_D10_1
59 ^(1 2)	59 ^(1 2)	61	61	92	92	PB6	I/O	-	PB6	TIM4_CH1/I2C_SCL/ USBHS2_DM/DVP_D5 ⁽⁷⁾	TIM8_CH1_1/ USART1_TX_1/ USART7_CTS_2/
60 ⁽¹⁾	60 ⁽¹⁾	62	62	93	93	PB7	I/O	-	PB7	TIM4_CH2/I2C_S	TIM8_CH2_1/

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
2)	2)									DA/ USBHS2_DP/FSM C_NADV	USART1_RX_1/ USART7_RTS_2/ FSMC_NADV_1
-	-	63	63	94	94	PE12	I/O	FT	PE12 BOOT0	BOOT0/USART10 _CK	USART4_CK_2/ USART4_CK_3/ USART10_CK_1/
61	61	64	64	95	95	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_ D4/ DVP_D6	TIM1_CH3_3/ TIM8_CH3_1/ USART4_CTS_2/ USART4_CTS_3/ USART5_CTS_1/ USART6_TX_1/ USART10_TX_1/ I2C_SCL_1/ LTDC_HSYNC_1/ CAN_RX_2/ SDIO_D4_1/ DVP_D6_1
62	62	65	65	96	96	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_ D5/ DVP_D7	TIM8_BKIN_1/ USART4_RTS_2/ USART4_RTS_3/ USART5_RTS_1/ USART6_RX_1/ USART10_RX_1/ I2C_SDA_1/ LTDC_VSYNC_1/ CAN_TX_2/ SDIO_D5_1/ DVP_D7_1
-	-	66	66	97	97	PE0	I/O	FT	PE0	TIM4_ETR/ USART10_TX/ FSMC_NBL0/LTD C_DE	TIM4_ETR_1/ USART4_TX_2/ USART4_TX_3/ USART6_CTS_1/ FSMC_NBL0_1
-	-	67	67	98	98	PE1	I/O	FT	PE1	USART10_RX/ FSMC_NBL1/LTD C_CLK	USART4_RX_2/ USART4_RX_3/ USART6_RTS_1/ FSMC_NBL1_1

Pin No.						Pin name	Pin type ⁽¹⁾	I/O structure	Main function (after reset)	Default alternate function	Remapping function ⁽⁹⁾
CH32V467RET6	CH32V407RET6	CH32V467WEU6	CH32V407WEU6	CH32V467VET6	CH32V407VET6						
63	63	-	-	99	99	V _{SS}	P	-	V _{SS}		
64	64	68	68	100	100	V _{DD}	P	-	V _{DD}		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input; *O* = CMOS tri-state output;

A = Analog signal input or output; *P* = power; *ETH* = Ethernet signal;

FT = 5V tolerance; *HS* = Support 100MHz high-speed.

Note 2: Both V_{DD} and V_{BAT} can be connected with an internal analog switch to supply power to the backup area and the pins PC13, PC14 and PC15. This analog switch can only pass a limited current (3mA). When powered by V_{DD} , PC14 and PC15 can be used for GPIO or LSE pins, and PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; PC13, PC14, and PC15 can only operate at frequencies below 2MHz when used as GPIO output pins, with a maximum load capacitance of 30pF. They cannot be used as current sources (e.g., to drive LEDs). When the power is supplied by V_{BAT} , PC14 and PC15 can only be used for LSE pin, and PC13 can be used as TAMPER pin, RTC alarm clock or second output;

Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32FV2x_V3xRM;

Note 4: For the CH32V407WEU6, CH32V407RET6, CH32V467WEU6, and CH32V467RET6 chips, pins 5 and 6 are configured by default as OSC_IN and OSC_OUT after chip reset. The software can reconfigure these two pins as PD0 and PD1; in this case, PD0 and PD1 are non-FT pins. However, for the CH32V407VET6 and CH32V467VET6 chips, since PD0 and PD1 are inherent function pins, there is no need for software remapping; in this case, PD0 and PD1 are FT pins. For more detailed information, please refer to the "Multifunction I/O" and "Debug Settings" sections of the CH32FV407RM.

Note 5: For chips where neither the BOOT0/PE12 nor the BOOT1/PB2 pins are brought out, the internal BOOT0/PE12 pin is shorted to VSS, while the BOOT1/PB2 pin is left floating. In low-power modes, it is recommended to configure PE12 and PB2 as pull-down input modes to prevent the generation of additional current.

For chips where the BOOT1/PB2 pin is exposed but the BOOT0/PE12 pin is not, the internal BOOT0/PE12 pin is shorted to VSS. In low-power modes, it is recommended to configure the PE12 input mode as a pull-down to prevent additional current draw.

For chips where the BOOT0/PE12 pins are brought out but the BOOT1/PB2 pins are not, the internal BOOT1/PB2 pins are internally shorted to VSS. In low-power conditions, it is recommended to configure the PB2 pin as a pull-down input to prevent additional current consumption.

A pull-down resistor should be connected to the BOOT0/PE12 pin to ensure that BOOT0 remains at a low level during power-up, allowing the device to enter boot mode in program flash memory. Once normal

operation has begun, the PE12 pin can be used for output as needed.

Note 6: SDIO_D0 and SDIO_D1 are mapped to PC8 and PC9 by default. When bit [14] (ETHMACEN) and bit [10] (SDIOEN) of the RCC_HBPCENR register are both set to 1, the default mapping of SDIO_D0 and SDIO_D1 automatically changes to PB14 and PB15.

Note 7: DVP_D5 is mapped to PB6 by default. When bit [13] (DVPEN) of the RCC_HBPCENR register is set to 1, bit [11] (USBHS1EN) is set to 1, and bit [2] (RB_UD_RST_SIE) of the R8_USB_CTRL register is set to 0, the default mapping of DVP_D5 automatically changes to PB3.

Note 8: FSMC_NADV is mapped to PB7 by default. When bit [8] FSMCEN in the RCC_HBPCENR register is set to 1, bit [11] USBHS2EN is set to 1, and bit [2] RB_UD_RST_SIE in the R8_USB_CTRL register is set to 0, the default mapping of FSMC_NADV automatically changes to PD2.

Note 9: In remapping mode, the value following the underscore indicates the configuration value of the corresponding bit in the AFIO register. For example, UART4_RX_3 indicates that the corresponding bit in the AFIO register is configured as 11b.

Note 10: TIM2_CH1 and TIM2_ETR share the same pin, but cannot be used simultaneously.

Note 11: Supports RX/TX transmission/reception identification and pair swapping for Ethernet pins; supports MDIRP/MDIRN polarity identification and swapping; supports MDITP/MDITN polarity identification and swapping.

Note 12: The CH32V407RET6 and CH32V467RET6 do not support USBHS2.

2.3 Pin Alternate Function

Note that the pin function descriptions in the following table are for all functions and do not relate to specific models. There are differences in peripheral resources between different models, please check whether this function is available according to the product model resource table before checking.

Table 2-2 Pin alternate and remapping functions

Pin	Alternate	ADC	TIM1/8	TIM2/3/4/5	USART1/2/3/4/5	USART6/7/8/9/10	SYS	I2C I3C	SPI I2S	USB	ETH	FSMC SDIO	LTDC	DVP	OPA	CAN
PA0		ADC_IN0	TIM8_ETR TIM8_ETR_1	TIM2_CH1 TIM2_ETR TIM2_CH1_2 TIM2_ETR_2 TIM5_CH1	USART2_CTS		WKUP									
PA1		ADC_IN1		TIM2_CH2 TIM2_CH2_2 TIM5_CH2	USART2_RTS								LTDC_R4 LTDC_R4_1			
PA2		ADC_IN2		TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX								LTDC_R5 LTDC_R5_1			
PA3		ADC_IN3		TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX								LTDC_R6 LTDC_R6_1			
PA4		ADC_IN4 DAC1_O UT			USART2_CK	USART9_TX_1			SPI1_NSS SPI3_NSS_1 I2S3_WS_1				LTDC_G5_1	DVP_HSYNC DVP_HSYNC_1		
PA5		ADC_IN5 DAC2_O UT			USART1_CK_3 USART1_CTS_2	USART6_CK_3 USART9_RX_1			SPI1_SCK					DVP_VSYNC DVP_VSYNC_1	OPA_N2	
PA6		ADC_IN6	TIM1_BKIN_1 TIM8_BKIN	TIM3_CH1	USART1_TX_3	USART7_TX_1			SPI1_MISO					DVP_PCLK DVP_PCLK_1	OPA_P2	
PA7		ADC_IN7	TIM1_CH1N_1 TIM8_CH1N TIM1_CH4_3	TIM3_CH2	USART1_RX_3	USART7_RX_1 USART8_CK			SPI1_MOSI				LTDC_R7 LTDC_R7_1		OPA_OUT1	
PA8			TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1 USART1_RX_2	USART7_CK_2 USART7_CK_3	MCO		I2S3_MCK				LTDC_B4 LTDC_B4_1	DVP_D2_1		
PA9			TIM1_CH2 TIM1_CH2_1		USART1_TX USART1_RTS_2	USART7_TX_2 USART7_TX_3						SDIO_D6_1	LTDC_DE_1	DVP_D0 DVP_D0_1		
PA10			TIM1_CH3 TIM1_CH3_1		USART1_CK_2 USART1_RX	USART7_RX_2 USART7_RX_3						SDIO_D7_1	LTDC_CLK_1	DVP_D1 DVP_D1_1		
PA11			TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1					USB1_DM						CAN_RX

Pin	Alternate	ADC	TIM1/8	TIM2/3/4/5	USART1/2/3/4/5	USART6/7/8/9/10	SYS	I2C I3C	SPI I2S	USB	ETH	FSMC SDIO	LTDC	DVP	OPA	CAN
PA12			TIM1_ETR TIM1_ETR_1		USART1_RTS USART1_RTS_1					USB1_DP						CAN_TX
PA13			TIM8_CH1N_1		USART3_TX_2 USART4_CTS	USART6_CK_2	SWDIO SWIO						LTDC_B5 LTDC_B5_1			
PA14			TIM8_CH2N_1		USART3_RX_2	USART6_CTS_2 USART8_TX_1	SWCLK						LTDC_B6 LTDC_B6_1			
PA15			TIM8_CH3N_1	TIM2_CH1_1 TIM2_ETR_1 TIM2_CH1_3 TIM2_ETR_3		USART6_RTS_2 USART8_RX_1			SPI1_NSS_1 SPI3_NSS I2S3_WS				LTDC_B7 LTDC_B7_1			
PB0		ADC_IN8	TIM1_CH2N_1 TIM8_CH2N	TIM3_CH3 TIM3_CH3_2	USART4_TX_1 USART5_CTS_2 USART5_CTS_3	USART6_CK USART7_CK_1 USART8_CTS							LTDC_G2 LTDC_G2_1			
PB1		ADC_IN9	TIM1_CH3N_1 TIM8_CH3N	TIM3_CH4 TIM3_CH4_2	USART4_RX_1 USART5_RTS_2 USART5_RTS_3	USART8_RTS USART9_TX							LTDC_G3 LTDC_G3_1		OPA_OU T2	
PB2					USART4_CK_1 USART5_CK_2 USART5_CK_3	USART9_RX	BOOT1						LTDC_G4			
PB3				TIM2_CH2_1 TIM2_CH2_3	USART5_CK_1 USART5_CTS				SPI1_SCK_1 SPI3_SCK I2S3_CK				LTDC_G4_1	DVP_D5 DVP_D5_1		
PB4				TIM3_CH1_2	USART5_TX_1 USART5_RTS			I3C_SCL_1	SPI1_MISO_1 SPI3_MISO				LTDC_HSYNC	DVP_D3_1		
PB5				TIM3_CH2_2	USART5_CK USART5_RX_1	USART6_CK_1		I2C_SMBA I3C_SDA_1	SPI1_MOSI_1 SPI3_MOSI I2S3_SD				LTDC_VSYNC	DVP_D10_1		
PB6			TIM8_CH1_1	TIM4_CH1	USART1_TX_1	USART7_CTS_2		I2C_SCL		USB2_D M				DVP_D5		
PB7			TIM8_CH2_1	TIM4_CH2	USART1_RX_1	USART7_RTS_2		I2C_SDA		USB2_DP		FSMC_NADV FSMC_NADV_1				
PB8			TIM8_CH3_1 TIM1_CH3_3	TIM4_CH3	USART4_CTS_2 USART4_CTS_3 USART5_CTS_1	USART6_TX_1 USART10_TX_1		I2C_SCL_1				SDIO_D4 SDIO_D4_1	LTDC_HSYNC_1	DVP_D6 DVP_D6_1		CAN_RX_2
PB9			TIM8_BKIN_1	TIM4_CH4	USART4_RTS_2 USART4_RTS_3 USART5_RTS_1	USART6_RX_1 USART10_RX_1		I2C_SDA_1				SDIO_D5 SDIO_D5_1	LTDC_VSYNC_1	DVP_D7 DVP_D7_1		CAN_TX_2
PB10			TIM1_BKIN_3	TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I3C_SCL					LTDC_B3 LTDC_B3_1			
PB11				TIM2_CH4_2 TIM2_CH4_3	USART3_RX	USART8_CK_2 USART8_CK_3		I3C_SDA				FSMC_D9 FSMC_D9_1	LTDC_B2 LTDC_B2_1			
PB12			TIM1_BKIN		USART3_CK	USART8_RTS_2 USART8_RTS_3			SPI2_NSS I2S2_WS			FSMC_D10 FSMC_D10_1	LTDC_G6 LTDC_G6_1		OPA_P1	
PB13			TIM1_CH1N		USART3_CTS USART3_CTS_1	USART8_CTS_2 USART8_CTS_3			SPI2_SCK I2S2_CK			FSMC_D11 FSMC_D11_1	LTDC_G7 LTDC_G7_1		OPA_N1	

Pin	Alternate	ADC	TIM1/8	TIM2/3/4/5	USART1/2/3/4/5	USART6/7/8/9/10	SYS	I2C I3C	SPI I2S	USB	ETH	FSMC SDIO	LTDC	DVP	OPA	CAN
PB14			TIM1_CH2N		USART3_RTS USART3_RTS_1	USART8_RX_2 USART8_RX_3			SPI2_MISO			FSMC_D12 FSMC_D12_1 SDIO_D0 SDIO_D0_1	LTDC_B0 LTDC_B0_1			
PB15			TIM1_CH3N		USART1_TX_2	USART8_CK_1 USART8_TX_2 USART8_TX_3			SPI2_MOSI I2S2_SD			SDIO_D1 SDIO_D1_1	LTDC_B1 LTDC_B1_1			
PC0		ADC_IN1 0				USART6_TX USART6_TX_3							LTDC_R0 LTDC_R0_1			
PC1		ADC_IN1 1				USART6_RX USART6_RX_3 USART7_CK							LTDC_R1 LTDC_R1_1			
PC2		ADC_IN1 2				USART6_CTS USART6_CTS_3 USART7_TX							LTDC_R2 LTDC_R2_1			
PC3		ADC_IN1 3				USART6_RTS USART6_RTS_3 USART7_RX							LTDC_R3 LTDC_R3_1			
PC4		ADC_IN1 4			USART1_CTS_3 USART4_CTS_1	USART7_CTS USART7_CTS_1 USART8_TX						FSMC_D4_1	LTDC_G0 LTDC_G0_1			
PC5		ADC_IN1 5			USART1_RTS_3 USART4_RTS_1	USART7_RTS USART7_RTS_1 USART8_RX							LTDC_G1 LTDC_G1_1			
PC6			TIM8_CH1	TIM3_CH1_3					I2S2_MCK			SDIO_D6				
PC7			TIM8_CH2	TIM3_CH2_3					I2S3_MCK			SDIO_D7				
PC8			TIM8_CH3	TIM3_CH3_3		USART7_CTS_3						SDIO_D0		DVP_D2		
PC9			TIM8_CH4	TIM3_CH4_3		USART7_RTS_3						SDIO_D1		DVP_D3		
PC10					USART3_TX_1 USART4_TX				SPI3_SCK_1 I2S3_CK_1			SDIO_D2 SDIO_D2_1		DVP_D8 DVP_D8_1		
PC11					USART3_RX_1 USART4_RX				SPI3_MISO_1			SDIO_D3 SDIO_D3_1		DVP_D4 DVP_D4_1		
PC12					USART3_CK_1 USART4_CK USART5_TX				SPI3_MOSI_1 I2S3_SD_1			SDIO_CK SDIO_CK_1		DVP_D9 DVP_D9_1		
PC13			TIM8_CH4_1				TAMPER-R TC									
PC14						USART10_CTS USART10_CTS_1	OSC32_IN									
PC15						USART10_RTS USART10_RTS_1	OSC32_OUT									
PD0							OSC_IN					FSMC_D2 FSMC_D2_1				CAN_RX_3
PD1							OSC_OUT					FSMC_D3 FSMC_D3_1				CAN_TX_3

Pin	Alternate	ADC	TIM1/8	TIM2/3/4/5	USART1/2/3/4/5	USART6/7/8/9/10	SYS	I2C I3C	SPI I2S	USB	ETH	FSMC SDIO	LTDC	DVP	OPA	CAN
PD2				TIM3_ETR TIM3_ETR_1 TIM3_ETR_2	USART4_RTS USART5_RX							SDIO_CMD SDIO_CMD_1 FSMC_NADV FSMC_NADV_1		DVP_D11 DVP_D11_1		
PD3					USART2_CTS_1							FSMC_CLK FSMC_CLK_1				
PD4					USART2_RTS_1							FSMC_NOE FSMC_NOE_1				
PD5					USART2_TX_1							FSMC_NWE FSMC_NWE_1				
PD6					USART2_RX_1							FSMC_NWAIT FSMC_NWAIT_1		DVP_D10		
PD7					USART2_CK_1							FSMC_NE1 FSMC_NE1_1 FSMC_NCE2 FSMC_NCE2_1				
PD8					USART3_TX_3	USART9_CK USART9_CK_1						FSMC_D13 FSMC_D13_1	LTDC_G5			
PD9					USART3_RX_3							FSMC_D14 FSMC_D14_1				
PD10					USART3_CK_2 USART3_CK_3	USART10_CK_2 USART10_CK_3						FSMC_D15 FSMC_D15_1				
PD11					USART3_CTS_2 USART3_CTS_3	USART10_TX_2 USART10_TX_3						FSMC_A16 FSMC_A16_1				
PD12				TIM4_CH1_1	USART3_RTS_2 USART3_RTS_3	USART10_RX_2 USART10_RX_3						FSMC_A17 FSMC_A17_1				
PD13				TIM4_CH2_1		USART10_CTS_2 USART10_CTS_3						FSMC_A18 FSMC_A18_1				
PD14				TIM4_CH3_1		USART10_RTS_2 USART10_RTS_3					LED0_1	FSMC_D0 FSMC_D0_1				
PD15				TIM4_CH4_1							LED1_1	FSMC_D1 FSMC_D1_1				
PE0				TIM4_ETR TIM4_ETR_1	USART4_TX_2 USART4_TX_3	USART6_CTS_1 USART10_TX						FSMC_NBL0 FSMC_NBL0_1	LTDC_DE			
PE1					USART4_RX_2 USART4_RX_3	USART6_RTS_1 USART10_RX						FSMC_NBL1 FSMC_NBL1_1	LTDC_CLK			
PE2						USART9_CK_2 USART9_CK_3						FSMC_A23 FSMC_A23_1				
PE3						USART9_TX_2 USART9_TX_3						FSMC_A19 FSMC_A19_1				
PE4						USART9_RX_2 USART9_RX_3						FSMC_A20 FSMC_A20_1				
PE5						USART9_CTS_2 USART9_CTS_3						FSMC_A21 FSMC_A21_1				

Pin \ Alternate	ADC	TIM1/8	TIM2/3/4/5	USART1/2/3/4/5	USART6/7/8/9/10	SYS	I2C I3C	SPI I2S	USB	ETH	FSMC SDIO	LTDC	DVP	OPA	CAN
PE6					USART9_RTS_2 USART9_RTS_3						FSMC_A22 FSMC_A22_1				
PE7		TIM1_ETR_3									FSMC_D4				
PE8		TIM1_CH1N_3		USART5_TX_2 USART5_TX_3	USART9_CTS USART9_CTS_1					LED0	FSMC_D5 FSMC_D5_1				
PE9		TIM1_CH1_3		USART5_RX_2 USART5_RX_3	USART9_RTS USART9_RTS_1					LED1	FSMC_D6 FSMC_D6_1				
PE10		TIM1_CH2N_3			USART6_TX_2 USART8_CTS_1						FSMC_D7 FSMC_D7_1				
PE11		TIM1_CH2_3			USART6_RX_2 USART8_RTS_1						FSMC_D8 FSMC_D8_1				
PE12		TIM1_CH3N_3		USART4_CK_2 USART4_CK_3	USART10_CK USART10_CK_1	BOOT0									

Table 2-3-1 ADC Pin functions

ADC function	Default pin
ADC_IN0	PA0
ADC_IN1	PA1
ADC_IN2	PA2
ADC_IN3	PA3
ADC_IN4	PA4
ADC_IN5	PA5
ADC_IN6	PA6
ADC_IN7	PA7
ADC_IN8	PB0
ADC_IN9	PB1
ADC_IN10	PC0
ADC_IN11	PC1
ADC_IN12	PC2
ADC_IN13	PC3
ADC_IN14	PC4
ADC_IN15	PC5
ADC_IN16	Temperature sensor
ADC_IN17	Internal reference voltage V_{REFINT}

Table 2-3-2 DAC Pin functions

DAC1 function	Default pin
DAC1_OUT	PA4
DAC2 function	Default pin
DAC2_OUT	PA5

Table 2-3-3 TIM Pin functions

TIM1 function	TIM1_RM=00 Default mapping pin	TIM1_RM=01 Remapping pin	TIM1_RM=11 Remapping pin
TIM1_ETR	PA12	PA12	PE7
TIM1_CH1	PA8	PA8	PE9
TIM1_CH2	PA9	PA9	PE11
TIM1_CH3	PA10	PA10	PB8
TIM1_CH4	PA11	PA11	PA7
TIM1_BKIN	PB12	PA6	PB10
TIM1_CH1N	PB13	PA7	PE8
TIM1_CH2N	PB14	PB0	PE10
TIM1_CH3N	PB15	PB1	PE12

TIM8 function	TIM8_RM=0 Default mapping pin		TIM8_RM=1 Remapping pin	
TIM8_ETR	PA0		PA0	
TIM8_CH1	PC6		PB6	
TIM8_CH2	PC7		PB7	
TIM8_CH3	PC8		PB8	
TIM8_CH4	PC9		PC13	
TIM8_BKIN	PA6		PB9	
TIM8_CH1N	PA7		PA13	
TIM8_CH2N	PB0		PA14	
TIM8_CH3N	PB1		PA15	
TIM2 function	TIM2_RM=00 Default mapping pin	TIM2_RM=01 Remapping pin	TIM2_RM=10 Remapping pin	TIM2_RM=11 Remapping pin
TIM2_ETR	PA0	PA15	PA0	PA15
TIM2_CH1	PA0	PA15	PA0	PA15
TIM2_CH2	PA1	PB3	PA1	PB3
TIM2_CH3	PA2	PA2	PB10	PB10
TIM2_CH4	PA3	PA3	PB11	PB11
TIM3 function	TIM3_RM=00 Default mapping pin		TIM3_RM=10 Remapping pin	TIM3_RM=11 Remapping pin
TIM3_ETR	PD2		PD2	PD2
TIM3_CH1	PA6		PB4	PC6
TIM3_CH2	PA7		PB5	PC7
TIM3_CH3	PB0		PB0	PC8
TIM3_CH4	PB1		PB1	PC9
TIM4 function	TIM4_RM=0 Default mapping pin		TIM4_RM=1 Remapping pin	
TIM4_ETR	PE0		PE0	
TIM4_CH1	PB6		PD12	
TIM4_CH2	PB7		PD13	
TIM4_CH3	PB8		PD14	
TIM4_CH4	PB9		PD15	
TIM5 function	Default pin			
TIM5_CH1	PA0			
TIM5_CH2	PA1			
TIM5_CH3	PA2			
TIM5 function	TIM5CH4_RM=0 Default mapping pin		TIM5CH4_RM=1 Remapping pin	

TIM5_CH4	PA3	LSI internal clock
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Table 2-3-4 USART Pin functions

USART1 function	USART1_RM1=0 ⁽¹⁾ USART1_RM=0 ⁽²⁾ Default mapping pin	USART1_RM1=0 ⁽¹⁾ USART1_RM=0 ⁽²⁾ Remapping pin	USART1_RM1=0 ⁽¹⁾ USART1_RM=0 ⁽²⁾ Remapping pin	USART1_RM1=0 ⁽¹⁾ USART1_RM=0 ⁽²⁾ Remapping pin
USART1_CK	PA8		PA10	PA5
USART1_TX	PA9	PB6	PB15	PA6
USART1_RX	PA10	PB7	PA8	PA7
USART1_CTS	PA11		PA5	PC4
USART1_RTS	PA12		PA9	PC5
USART2 function	USART2_RM=0 Default mapping pin		USART2_RM=1 Remapping pin	
USART2_CK	PA4		PD7	
USART2_TX	PA2		PD5	
USART2_RX	PA3		PD6	
USART2_CTS	PA0		PD3	
USART2_RTS	PA1		PD4	
USART3 function	USART3_RM=00 Default mapping pin	USART3_RM=01 Remapping pin	USART3_RM=10 Remapping pin	USART3_RM=11 Remapping pin
USART3_CK	PB12	PC12	PD10	
USART3_TX	PB10	PC10	PA13	PD8
USART3_RX	PB11	PC11	PA14	PD9
USART3_CTS	PB13		PD11	
USART3_RTS	PB14		PD12	
USART4 function	USART4_RM=00 Default mapping pin		USART4_RM=01 Remapping pin	USART4_RM=1x Remapping pin
USART4_CK	PC12		PB2	PE12
USART4_TX	PC10		PB0	PE0
USART4_RX	PC11		PB1	PE1
USART4_CTS	PA13		PC4	PB8
USART4_RTS	PD2		PC5	PB9
USART5 function	USART5_RM=00 Default mapping pin		USART5_RM=01 Remapping pin	USART5_RM=1x Remapping pin
USART5_CK	PB5		PB3	PB2
USART5_TX	PC12		PB4	PE8
USART5_RX	PD2		PB5	PE9

USART5_CTS	PB3		PB8		PB0	
USART5_RTS	PB4		PB9		PB1	
USART6 function	USART6_RM=00 Default mapping pin	USART6_RM=01 Remapping pin	USART6_RM=10 Remapping pin		USART6_RM=11 Remapping pin	
USART6_CK	PB0	PB5	PA13		PA5	
USART6_TX	PC0	PB8	PE10		PC0	
USART6_RX	PC1	PB9	PE11		PC1	
USART6_CTS	PC2	PE0	PA14		PC2	
USART6_RTS	PC3	PE1	PA15		PC3	
USART7 function	USART7_RM=00 Default mapping pin	USART7_RM=01 Remapping pin	USART7_RM=10 Remapping pin		USART7_RM=11 Remapping pin	
USART7_CK	PC1	PB0	PA8			
USART7_TX	PC2	PA6	PA9			
USART7_RX	PC3	PA7	PA10			
USART7_CTS	PC4			PB6		PC8
USART7_RTS	PC5			PB7		PC9
USART8 function	USART8_RM=00 Default mapping pin		USART8_RM=01 Remapping pin		USART8_RM=1x Remapping pin	
USART8_CK	PA7		PB15		PB11	
USART8_TX	PC4		PA14		PB15	
USART8_RX	PC5		PA15		PB14	
USART8_CTS	PB0		PE10		PB13	
USART8_RTS	PB1		PE11		PB12	
USART9 function	USART9_RM=00 Default mapping pin		USART9_RM=01 Remapping pin		USART9_RM=1x Remapping pin	
USART9_CK	PD8				PE2	
USART9_TX	PB1		PA4		PE3	
USART9_RX	PB2		PA5		PE4	
USART9_CTS	PE8				PE5	
USART9_RTS	PE9				PE6	
USART10 function	USART10_RM=00 Default mapping pin		USART10_RM=01 Remapping pin		USART10_RM=1x Remapping pin	
USART10_CK	PE12				PD10	
USART10_TX	PE0		PB8		PD11	
USART10_RX	PE1		PB9		PD12	
USART10_CTS	PC14				PD13	
USART10_RTS	PC15				PD14	

Note: 1. *USART1_RM* is bit 2 of the *AFIO_PCFR1* register, representing the low-order bit of the mapping configuration.

2. *USART1_RM1* is bit 26 of the *AFIO_PCFR2* register, representing the high-order bit of the mapping configuration.

Table 2-3-5 SPI and I2S Pin functions

SPI1 function	SPI1_RM=0 Default mapping pin	SPI1_RM=1 Remapping pin
SPI1_NSS	PA4	PA15
SPI1_SCK	PA5	PB3
SPI1_MISO	PA6	PB4
SPI1_MOSI	PA7	PB5
SPI2 and I2S2 function	Default pin	
SPI2_NSS/I2S2_WS	PB12	
SPI2_SCK/I2S2_CK	PB13	
SPI2_MISO	PB14	
I2S2_MCK	PC6	
SPI2_MOSI/I2S2_SD	PB15	
SPI3 and I2S3 function	SPI3_RM=0/I2S3_RM=0 Default mapping pin	SPI3_RM=1/I2S3_RM=1 Remapping pin
SPI3_NSS/I2S3_WS	PA15	PA4
SPI3_SCK/I2S3_CK	PB3	PC10
SPI3_MISO	PB4	PC11
I2S3_MCK	PC7	PC7
SPI3_MOSI/I2S3_SD	PB5	PC12

Table 2-3-6 I2C Pin functions

I2C function	I2C_RM=0 Default mapping pin	I2C_RM=1 Remapping pin
I2C_SCL	PB6	PB8
I2C_SDA	PB7	PB9
I2C_SMBA	PB5	

Table 2-3-7 I3C Pin functions

I3C function	I3C_RM=0 Default mapping pin	I3C_RM=1 Remapping pin
I3C_SCL	PB10	PB4
I3C_SDA	PB11	PB5

Table 2-3-8 FSMC Pin Functions

FSMC function	FSMC_RM=0 Default mapping pin	FSMCEN=1&USBHS2EN=1 &RB_UD_RST_SIE=0	FSMC_RM=1 Remapping pin
FSMC_NBL0	PE0	PE0	PE0
FSMC_NBL1	PE1	PE1	PE1
FSMC_CLK	PD3	PD3	PD3
FSMC_NOE	PD4	PD4	PD4
FSMC_NWE	PD5	PD5	PD5
FSMC_NWAIT	PD6	PD6	PD6
FSMC_NE1/FSMC_NCE2	PD7	PD7	PD7
FSMC_NADV	PB7	PD2	PB7
FSMC_A16	PD11	PD11	PD11
FSMC_A17	PD12	PD12	PD12
FSMC_A18	PD13	PD13	PD13
FSMC_A19	PE3	PE3	PE3
FSMC_A20	PE4	PE4	PE4
FSMC_A21	PE5	PE5	PE5
FSMC_A22	PE6	PE6	PE6
FSMC_A23	PE2	PE2	PE2
FSMC_D0	PD14	PD14	PD14
FSMC_D1	PD15	PD15	PD15
FSMC_D2	PD0	PD0	PD0
FSMC_D3	PD1	PD1	PD1
FSMC_D4	PE7	PE7	PC4
FSMC_D5	PE8	PE8	PE8
FSMC_D6	PE9	PE9	PE9
FSMC_D7	PE10	PE10	PE10
FSMC_D8	PE11	PE11	PE11
FSMC_D9	PB11	PB11	PB11
FSMC_D10	PB12	PB12	PB12
FSMC_D11	PB13	PB13	PB13
FSMC_D12	PB14	PB14	PB14
FSMC_D13	PD8	PD8	PD8
FSMC_D14	PD9	PD9	PD9
FSMC_D15	PD10	PD10	PD10

Table 2-3-9 DVP Pin Functions

DVP function	DVPEN=1,DVP_RM=0	DVPEN=1&USBHSEN=1	DVP_RM=1
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	Default mapping pin	&RB_UD_RST_SIE=0	Remapping pin
DVP_PCLK	PA6	PA6	PA6
DVP_VSYNC	PA5	PA5	PA5
DVP_HSYNC	PA4	PA4	PA4
DVP_D0	PA9	PA9	PA9
DVP_D1	PA10	PA10	PA10
DVP_D2	PC8	PC8	PA8
DVP_D3	PC9	PC9	PB4
DVP_D4	PC11	PC11	PC11
DVP_D5	PB6	PB3	PB3
DVP_D6	PB8	PB8	PB8
DVP_D7	PB9	PB9	PB9
DVP_D8	PC10	PC10	PC10
DVP_D9	PC12	PC12	PC12
DVP_D10	PD6	PD6	PB5
DVP_D11	PD2	PD2	PD2

Table 2-3-10 SDIO Pin Functions

SDIO function	SDIO_RM=0 Default mapping pin	SDIOEN=1ÐMACEN=1	SDIO_RM=1 Remapping pin
SDIO_CK	PC12	PC12	PC12
SDIO_CMD	PD2	PD2	PD2
SDIO_SD0	PC8	PB14	PB14
SDIO_SD1	PC9	PB15	PB15
SDIO_SD2	PC10	PC10	PC10
SDIO_SD3	PC11	PC11	PC11
SDIO_SD4	PB8	PB8	PB8
SDIO_SD5	PB9	PB9	PB9
SDIO_SD6	PC6	PC6	PA9
SDIO_SD7	PC7	PC7	PA10

Table 2-3-11 LTDC Pin Functions

LTDC function	LTDC_RM=0 Default mapping pin	LTDC_RM=1 Remapping pin
LTDC_CLK	PE1	PA10
LTDC_HSYNC	PB4	PB8
LTDC_VSYNC	PB5	PB9
LTDC_DE	PE0	PA9

LTDC_R0	PC0	PC0
LTDC_R1	PC1	PC1
LTDC_R2	PC2	PC2
LTDC_R3	PC3	PC3
LTDC_R4	PA1	PA1
LTDC_R5	PA2	PA2
LTDC_R6	PA3	PA3
LTDC_R7	PA7	PA7
LTDC_G0	PC4	PC4
LTDC_G1	PC5	PC5
LTDC_G2	PB0	PB0
LTDC_G3	PB1	PB1
LTDC_G4	PB2	PB3
LTDC_G5	PD8	PA4
LTDC_G6	PB12	PB12
LTDC_G7	PB13	PB13
LTDC_B0	PB14	PB14
LTDC_B1	PB15	PB15
LTDC_B2	PB11	PB11
LTDC_B3	PB10	PB10
LTDC_B4	PA8	PA8
LTDC_B5	PA13	PA13
LTDC_B6	PA14	PA14
LTDC_B7	PA15	PA15

Table 2-3-12 CAN Pin Functions

CAN function	CAN1_RM=00 Default mapping pin	CAN1_RM=10 Remapping pin	CAN1_RM=11 Remapping pin
CAN_RX	PA11	PB8	PD0
CAN_TX	PA12	PB9	PD1

Table 2-3-13 ETH PHY Pin Functions

ETH PHY function	ETHPHY_LED_RM=0 Default mapping pin	ETHPHY_LED_RM=1 Remapping pin
LED0	PE8	PD14
LED1	PE9	PD15

Table 2-3-14 OPA Pin Functions

OPA function	Option pins
OPA_P	PB12/OPA_P1, PA6/OPA_P2
OPA_N	PB13/OPA_N1, PA5/OPA_N2
OPA_OUT	PA7/OPA_OUT1, PB1/OPA_OUT2

Table 2-3-15 USBHS Pin Functions

USBHS1 function	Default pin
USBHS1_DP	PA12
USBHS1_DM	PA11
USBHS2 function	Default pin
USBHS2_DP	PB7
USBHS2_DM	PB6

Table 2-3-16 Debug Pin Functions

Debug pin function	Default pin
SWCLK	PA14
SWDIO/SWIO	PA13

Table 2-3-17 MCO Pin Functions

MCO function	Default pin
MCO	PA8

Chapter 3 Electrical Characteristics

3.1 Test Conditions

Unless otherwise specified and marked, all voltages are referenced to V_{SS} .

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency.

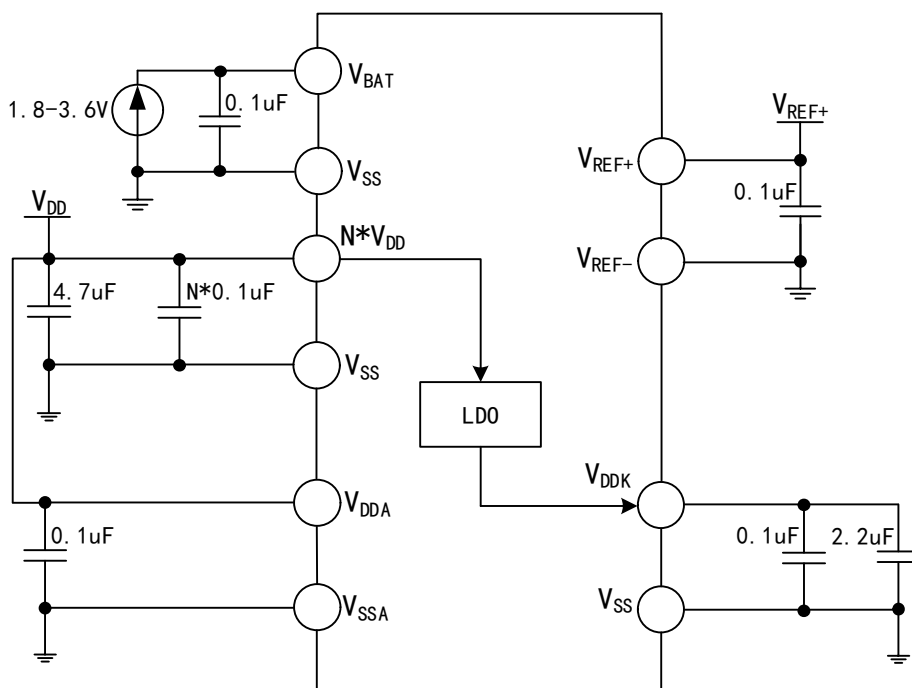
The typical values for the CH32V407 are provided as design guidelines based on an ambient temperature of 25°C, a supply voltage of $V_{DD} = V_{DDA} = 3.3V$, and a V_{DDK} of 1.2V.

The typical specifications for the CH32V467 are provided as a design guide based on an ambient temperature of 25°C, with a supply voltage of $V_{DD} = V_{DDA} = 3.3V$, resulting in $V_{DD18} = 1.8V$ and $V_{DDK} = 1.2V$.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

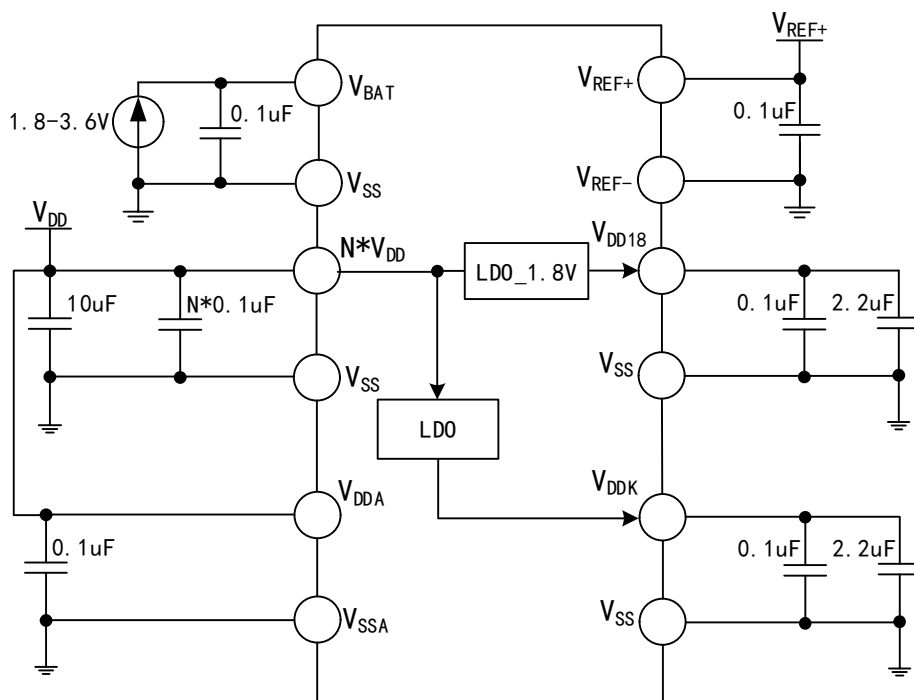
Figure 3-1-1 CH32V407 standard power supply typical circuit



Note: For the CH32V407 chip, there are multiple V_{DD} pins on the chip package; pins with the same name must be shorted together.

The main V_{DD} pin (adjacent to the Ethernet signal pin) should be connected to a 0.1uF decoupling capacitor in parallel with a capacitor of at least 4.7uF capacity; the remaining V_{DD} pins only need to be connected to a 0.1uF decoupling capacitor.

Figure 3-1-2 CH32V467 standard power supply typical circuit



Note: For the CH32V467 chip, there are multiple pins labeled V_{DD} on the chip package; power pins with the same name must be shorted together.

The main V_{DD} pin (adjacent to the Ethernet signal pins) should be connected to a decoupling capacitor consisting of a 0.1uF capacitor in parallel with a 10uF capacitor, with a total capacitance not less than the combined total capacitance of V_{DDK} and V_{DD18} . The remaining V_{DD} pins only need to be connected to a 0.1uF decoupling capacitor.

3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T _A	Ambient temperature during operation	-40	85	°C
T _S	Ambient temperature during storage	-40	125	°C
V _{DD}	External main supply voltage (including V _{DD} and V _{DDA})	-0.3	4.0	V
V _{DDK}	Power decoupling end of core circuit	-0.2	1.5	V
V _{REF+}	Positive reference voltage of ADC and DAC modules	-0.3	V _{DDA} +0.3	V
V _{IN}	Input voltage on FT (tolerant 5V) pin.	-0.3	5.5	V
	Input voltage on USB 2.0 and Ethernet PHY pins	-0.3	V _{DD} +0.3	V
	Input voltage on other pins (supplied by V _{DD})	-0.3	V _{DD} +0.3	V
ΔV _{DD_x}	Voltage difference between V _{DD} of main power supply pin		20	mV
ΔV _{SS_x}	Voltage difference between V _{SS} of common ground pin		20	mV
V _{ESDIO(HBM)}	ESD electrostatic discharge voltage (HBM) of I/O pin	4K		V
	USB pins (PA11, PA12, PB6, PB7)	4K		V
	ETH pin (MDI*)	4K		V

I_{VDD}	Total current of all V_{DD} main supply pins		250	mA
I_{VSS}	Total current of all V_{SS} common ground pins		250	mA
I_{IO}	Sink current on any I/O and control pin		25	mA
	Output current on any I/O and control pin		-25	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HCLK}	Internal HB clock frequency	LDO_VDDK[2:0] = 011(Default)			200 ⁽³⁾	MHz
		LDO_VDDK[2:0] = 100			240 ⁽⁴⁾	MHz
F_{PCLK1}	Internal PB1 clock frequency				F_{HCLK}	MHz
F_{PCLK2}	Internal PB2 clock frequency				F_{HCLK}	MHz
V_{DD}	Standard working voltage	USB or ETH not used.	2.9 ⁽⁵⁾	3.3	3.6	V
		Use USB or ETH	3.15	3.3	3.45	V
V_{DDA}	Analog part working voltage	V_{DDA} must be the same as V_{DD} ; V_{REF+} must not exceed V_{DD} ; V_{REF-} is equal to V_{SS} .	2.9	3.3	3.6	V
$V_{DDK}^{(1)}$	Core operating voltage		1.17	1.2	1.27	V
V_{DD18}	On-chip extended PSRAM working voltage		1.2	1.8	2.0	V
V_{BAT}	Working voltage of backup unit		1.8		3.6	V
$V_{REF+}^{(2)}$	Positive reference voltage of ADC and DAC modules	V_{REF+} must not exceed V_{DD} ; V_{REF-} is equal to V_{SS} .	2.4	3.3	3.6	V
T_A	Ambient temperature at work		-40		85	°C
T_J	Junction temperature		-40		105	°C

Note: 1. Since V_{DDK} draws a significant current, account for voltage drop losses in the PCB traces. If using an external power supply, add 10~50 mV to the 1.2V supply voltage.

2. The external capacitor connected to V_{REF+} should be placed as close as possible; otherwise, ADC performance may be affected.

3. Measured at room temperature, the frequency is no less than 240MHz; however, this does not account for temperature and process variations. The use of 240MHz is prohibited in production applications.

4. Suitable only for commercial-grade applications: $T_A \leq 70^\circ\text{C}$ and with adequate heat dissipation.

5. When the chip enters stop mode (LDO configured as low power consumption mode) or enters standby mode, V_{DD} cannot be lower than 3.0V.

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		20	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{PVD}^{(1)}$	Programmable voltage detector level selection	PLS[1:0] = 00 (rising edge)		2.85		V
		PLS[1:0] = 00 (falling edge)		2.81		V
		PLS[1:0] = 01 (rising edge)		2.94		V
		PLS[1:0] = 01 (falling edge)		2.90		V
		PLS[1:0] = 10 (rising edge)		3.04		V
		PLS[1:0] = 10 (falling edge)		3.00		V
		PLS[1:0] = 11 (rising edge)		3.14		V
		PLS[1:0] = 11 (falling edge)		3.10		V
$V_{PVDhyst}$	PVD hysteresis			0.04		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge		2.72		V
		Falling edge		2.69		V
$V_{PDRhyst}$	PDR hysteresis			30		mV
$t_{RSTTEMPO}$	Power on reset		16	28	30	ms
	Other reset		2	10	30	ms

Note: 1. Normal temperature test value.

3.3.3 Embedded Reference Voltage

Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$	1.17	1.2	1.23	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage		8			us

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2-1 CH32V407 Current consumption measurement

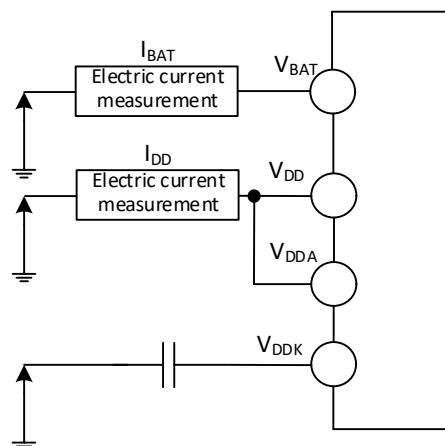
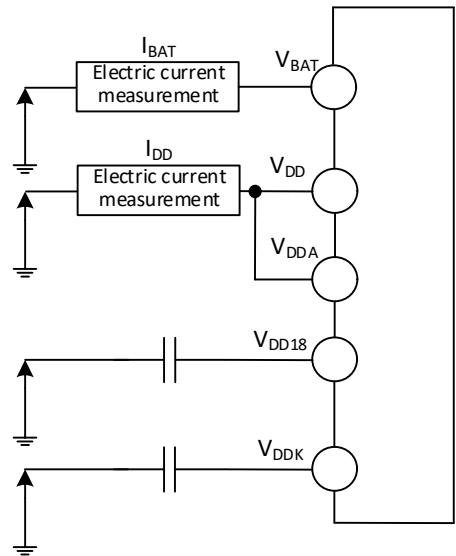


Figure 3-2-2 CH32V467 Current consumption measurement



CH32V407 is in the following conditions:
Under normal operating conditions ($V_{DD} = V_{DDA} = 3.3V$, $V_{DDK} = 1.2V$), during testing: Configure all I/O ports as pull-down inputs; enable only one of HSE or HSI; set HSE to 25MHz and HSI to 20MHz (calibrated); set F_{PCLK1} and F_{PCLK2} to F_{HCLK} ; enable the PLL when $F_{HCLK} > HSE$ or HSI. Measure the power consumption when enabling or disabling all peripheral clocks.

CH32V467 is in the following conditions:
Under normal operating conditions ($V_{DD} = V_{DDA} = 3.3V$, $V_{DD18} = 1.8V$, $V_{DDK} = 1.2V$), during testing: Configure all I/O ports as pull-down inputs; enable only one of HSE or HSI; set HSE to 25MHz and HSI to 20MHz (calibrated); set F_{PCLK1} and F_{PCLK2} to F_{HCLK} ; when $F_{HCLK} > HSE$ or HSI, the PLL is enabled. Measure the power consumption when enabling or disabling all peripheral clocks.

Table 3-6 Typical current consumption of CH32V407 in Run mode, and data processing code runs from internal flash memory

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I _{DD} ⁽¹⁾⁽²⁾	Supply current in Run mode	External clock	F _{HCLK} = 240MHz	47.5	25.0	mA
			F _{HCLK} = 200MHz	40.1	22.6	
			F _{HCLK} = 175MHz	35.3	19.6	
			F _{HCLK} = 120MHz	30.2	18.8	
			F _{HCLK} = 60MHz	15.8	10.3	
			F _{HCLK} =	6.1	3.8	

			20MHz			
		Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency.	F _{HCLK} = 240MHz	46.1	24.1	
			F _{HCLK} = 200MHz	39.1	21.5	
			F _{HCLK} = 175MHz	35.0	18.7	
			F _{HCLK} = 120MHz	24.2	13.0	
			F _{HCLK} = 60MHz	13.2	7.4	
			F _{HCLK} = 20MHz	4.5	2.6	

Note: 1. The above are the measured parameters for the CH32V407.

2. For the CH32V467 chip, current consumption in operating mode increases by 2~22mA compared to the values in the table above.

Table 3-7 Typical current consumption of CH32V407 in Sleep mode, data processing code runs from internal flash memory or SRAM.

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I _{DD} ⁽¹⁾⁽²⁾	Supply current in sleep mode (peripheral power supply and clock holding at this time)	External clock	F _{HCLK} = 240MHz	31.6	9.4	mA
			F _{HCLK} = 200MHz	25.5	7.8	
			F _{HCLK} = 175MHz	22.6	6.8	
			F _{HCLK} = 120MHz	21.4	6.5	
			F _{HCLK} = 60MHz	11.5	6.0	
			F _{HCLK} = 20MHz	4.2	2.9	
		Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency.	F _{HCLK} = 240MHz	30.7	8.6	
			F _{HCLK} = 200MHz	24.8	6.9	
			F _{HCLK} = 175MHz	21.7	6.0	
			F _{HCLK} = 120MHz	15.2	4.2	
	F _{HCLK} = 60MHz	8.5	3.0			

			F_{HCLK} 20MHz	=	2.9	1.1	
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Note: 1. The above are the measured parameters for the CH32V407.

2. For the CH32V467 chip, current consumption in operating mode increases by 2~22mA compared to the values in the table above.

Table 3-8 Typical current consumption of CH32V407 in Stop and Standby modes

Symbol	Parameter	Condition	Typ.	Unit
$I_{DD}^{(1)}$	Supply current in Stop mode ⁽³⁾	The voltage regulator is in the running mode, and the low-speed and high-speed internal RC oscillators and external oscillators are in the off state (no independent watchdog).	433	uA
		The voltage regulator is in the low power consumption mode ⁽²⁾ , the low-speed and high-speed internal RC oscillators and external oscillators are in the off state (PVD is off without independent watchdog), and the RAM enters the low power consumption mode.	173	
	Supply current in Standby mode ⁽³⁾	Low-speed internal RC oscillator and independent watchdog are turned on, and all RAM is not charged.	3.1	
		Low-speed internal RC oscillator is on, independent watchdog is off, and all RAM is not charged.	3.1	
		LSI/LSE/RTC/IWDG is turned off, and 32K_RAM is charged and in a low power consumption state.	2.9	
I_{DD_VBAT}	Supply current of backup area (V_{DD} and V_{DDA} are removed, and only V_{BAT} is used for power supply)	LSI/LSE/RTC/IWDG is turned off, and all RAM is not charged.	1.5	uA
		Low-speed external oscillator and RTC are turned on.	2.1	

Note: 1. The above are measured parameters.

2. For the CH32V467 chip with the fifth last digit of the lot number being 0, in stop mode (the voltage regulator is in low-power consumption mode), the bit LDO18_EN=0 in the register PWR_CTLR must be configured.

3. For CH32V467 chips, current consumption in stop mode increases by 90uA compared to the values in the table above.

4. For chips with the fifth last digit of the lot number being 0, before entering standby mode, the I/O pins not used for wake-up function must be configured as analog inputs.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		5	25	32	MHz
$V_{HSEH}^{(1)}$	OSC_IN input pin high level voltage		$0.8 \cdot V_{DD}$		V_{DD}	V
$V_{HSEL}^{(1)}$	OSC_IN input pin low-level voltage		0		$0.2 \cdot V_{DD}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current				± 1	μA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

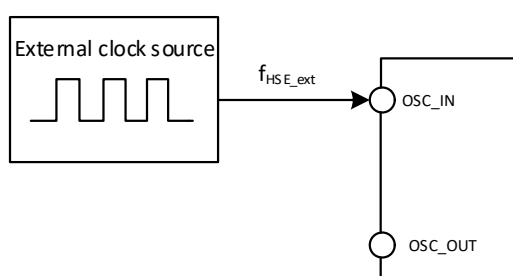


Table 3-10 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.8 \cdot V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		0		$0.2 \cdot V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current				± 1	μA

Figure 3-4 External low-frequency clock source circuit

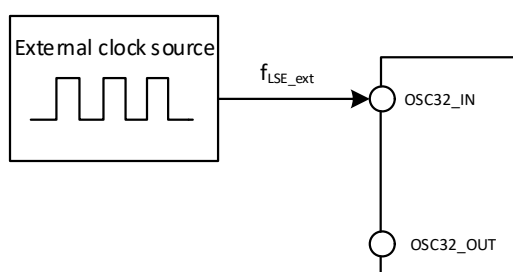


Table 3-11 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		5	25	32	MHz

R_F	Feedback resistance			250		k Ω
C	Recommended load capacitance and corresponding crystal series impedance R_S	$R_S=60\Omega^{(1)}$		20		pF
I_2	HSE drive current			0.53		mA
g_m	Oscillator transconductance	Startup		17		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} stable, 25M crystal		1 ⁽²⁾		ms

Note 1: It is recommended that the crystal's ESR does not exceed 80 Ω . Prioritize crystals with lower ESR values. Refer to the crystal manual for load capacitance requirements.

2. Start time refers to the time difference from HSEON being activated until HSERDY is set.

3. Ethernet or high-speed USB applications typically require an HSE; a 25MHz crystal is recommended, with a jitter of no more than 30ppm.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally $C_{L1}=C_{L2}$.

Figure 3-5 Typical circuit of external 25M crystal

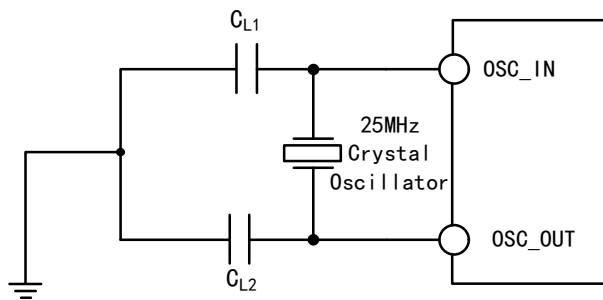


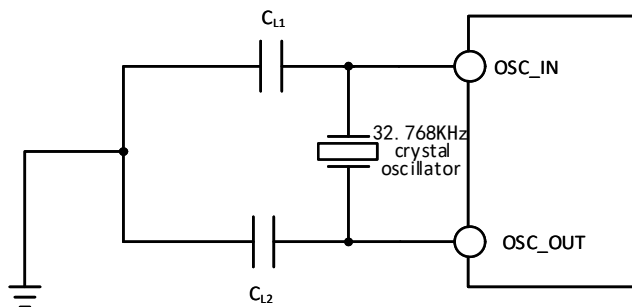
Table 3-12 Low-speed external clock generated by generated from a crystal/ceramic resonator
($f_{LSE}=32.768kHz$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback resistance			5		M Ω
C	Recommended load capacitance and corresponding crystal serial impedance R_S	$R_S<70k\Omega$			15	pF
i_2	LSE drive current	$V_{DD} = 3.3V$		0.35		μA
g_m	Oscillator transconductance	Startup		25.3		$\mu A/V$
$t_{SU(LSE)}$	Startup time	V_{DD} is stable		800		mS

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, usually $C_{L1}=C_{L2}$, which is about 12pF.

Figure 3-6 Typical circuit of external 32.768K crystal



Note: The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$. C_{stray} is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF.

3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			20		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	$T_A = 0^{\circ}\text{C} \sim 70^{\circ}\text{C}$	-1.6		1.6	%
		$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time ⁽¹⁾				8	us
$I_{DD(HSI)}$	HSI oscillator power consumption		140	200	280	uA

Note: 1. Set bit 1 of the `RCC_CTLR` register to `HSION` and wait for `HSIRDY` to be set to 1.

Table 3-14 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	40	60	kHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time ⁽¹⁾			230		us
$I_{DD(LSI)}$	LSI oscillator power consumption			1		uA

Note: 1. Set bit 1 of the `RCC_RSTSCKR` register to 1 and wait for `LSIRDY` to be set to 1.

3.3.7 PLL Characteristics

Table 3-15 PLL characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		5		32	MHz
	PLL input clock duty cycle		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		100		400	MHz
t_{LOCK}	PLL lock time			40	90	us

3.3.8 Wakeup Time from Low-power Mode

Table 3-16 Wakeup time from low-power mode⁽¹⁾

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	2.4	us
t_{wustop}	Wakeup from Stop mode (The voltage regulator is in running mode)	Wake up using HSI RC clock	23.1	us
	Wakeup from Stop mode (The voltage regulator is in low-power mode)	Wake-up time of voltage regulator from low power consumption mode+wake-up time of +HSIRC clock	76.7	
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO settling time+HSI RC clock wake-up+code loading time (1) (for example, 512K)	18.5	us

Note: 1. The code loading time can be calculated by the capacity of the waiting area of the current chip configuration 0 and the size of the loading configuration clock.

3.3.9 Memory Characteristics

Table 3-17 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) programming time	$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		1	15	ms
t_{erase_sec}	Sector (4K bytes) erase time	$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		2	50	ms
t_{erase_block}	Block (32K bytes) erase time	$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		16	200	ms

Note: Flash operation frequencies include read, program, and erase operations; the clock signal is derived from HCLK.

Table 3-18 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase times	$T_A = 25^{\circ}\text{C}$	50K			Times
t_{RET}	Data retention period		20			Years

3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		$0.41 \cdot (V_{*} - 1.8) + 1.3$		$V_{*} + 0.3$	V
	FT I/O pin, input high level voltage		$0.42 \cdot (V_{*} - 1.8) + 1$		5.0	V
V_{IL}	Standard I/O pin, input low level voltage		-0.3		$0.28 \cdot (V_{*} - 1.8) + 0.6$	V
	FT I/O pin, input low level voltage		-0.3		$0.32 \cdot (V_{*} - 1.8) + 0.55$	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis		150			mV

	FT I/O pin Schmitt trigger voltage hysteresis		90			
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Pull-up equivalent resistance		30	40	50	k Ω
R_{PD}	Pull-down equivalent resistance		30	40	50	k Ω
C_{IO}	I/O pin capacitance			5		pF

Note: I/O pins are powered by V_{DD} or V_{BAT} ; in the table above, V^* refers to either V_{DD} or V_{BAT} , depending on the specific pin.

Output drive current characteristics

GPIO (General-Purpose Input/Output) pins can handle input or output currents of up to $\pm 8\text{mA}$, and can handle input or output currents of $\pm 20\text{mA}$ (without strictly adhering to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-20-1 Output voltage characteristics (Excluding pins PC13~PC15)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 8 pins are sunk	CMOS port, $I_{IO} = 8\text{mA}$ $2.9\text{V} < V_{DD} < 3.6\text{V}$		0.4	V
V_{OH}	Output high level when 8 pins are sourced		$V_{DD}-0.4$		
V_{OL}	Output low level when 8 pins are sunk	$I_{IO} = 20\text{mA}$ $2.9\text{V} < V_{DD} < 3.6\text{V}$		1.0	V
V_{OH}	Output high level when 8 pins are sourced		$V_{DD}-1.2$		

Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 3-20-2 Output voltage characteristics (Refer to pins PC13~PC15)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 3 pins are sunk	$I_{IO} = +5\text{mA}$ $2.9\text{V} \leq V^* \leq 3.6\text{V}$		0.4	V
V_{OH}	Output high level when 3 pins are sourced	$I_{IO} = +1.5\text{mA}$ $2.9\text{V} \leq V^* \leq 3.6\text{V}$	$V^*-0.4$		

Note: In the table above, V^* may be represented as V_{DD} or V_{BAT} depending on the specific pin.

Table 3-21 Output AC characteristics (Excluding pins PC13~PC15)

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 (2MHz)	$F_{\max(IO)out}$	Maximum frequency	$CL=50\text{pF}$		2	MHz
	$t_{f(IO)out}$	Falling time of output high to low level	$CL=50\text{pF}$		125	ns
	$t_{r(IO)out}$	Rising time of output low to			125	ns

		high level				
01 (10MHz)	$F_{\max(\text{IO})\text{out}}$	Maximum frequency	CL=50pF		10	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Falling time of output high to low level	CL=50pF		25	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Rising time of output low to high level			25	ns
11 (50MHz)	$F_{\max(\text{IO})\text{out}}$	Maximum frequency	CL=10pF, no HS pin		70	MHz
			CL=30pF, no HS pin		50	MHz
			CL=50pF, no HS pin		30	MHz
			CL=10pF, HS pin		100	MHz
			CL=30pF, HS pin		75	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Falling time of output high to low level	CL=30pF		5	ns
			CL=50pF		8	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Falling time of output high to low level	CL=30pF		5	ns
			CL=50pF		8	ns
	$t_{\text{EXTI}pw}$	EXTI controller detects the pulse width of external signal		10		ns

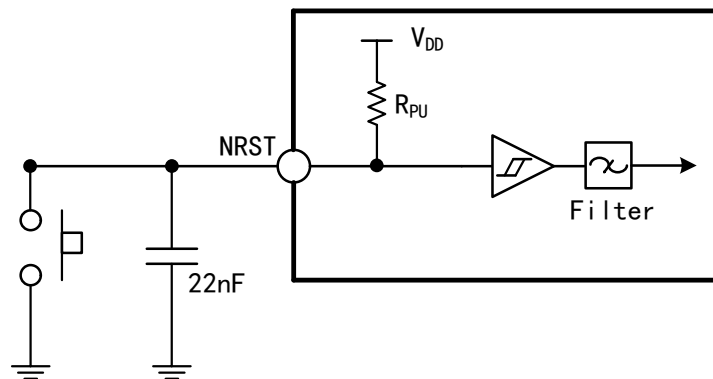
Note: 1. When used as GPIO output pins, PC13, PC14, and PC15 can only operate at frequencies below 2 MHz, with a maximum drive load of 30 pF.

2. The USB interface I/O complies only with the $MODEx[1:0]=10b$ or $01b$ parameter.

3.3.11 NRST Pin Characteristics

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin



Note: The capacitor shown in the diagram is optional and can be used to filter out key bounce.

Table 3-22 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{\text{IL}(\text{NRST})}$	NRST input low-level voltage		-0.3		$0.28 \cdot (V_{\text{DD}} - 1.8) + 0.6$	V
$V_{\text{IH}(\text{NRST})}$	NRST input high-level voltage		$0.41 \cdot (V_{\text{DD}} - 1.8) + 1.3$		$V_{\text{DD}} + 0.3$	V
$V_{\text{hys}(\text{NRST})}$	NRST Schmitt Trigger voltage hysteresis		150			mV
$R_{\text{PU}}^{(1)}$	Pull-up equivalent resistance		30	40	50	k Ω
$V_{\text{F}(\text{NRST})}$	NRST input filtered pulse width				100	ns

$V_{NF(NRST)}$	NRST input not filtered pulse width		300			ns
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Note: The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).

3.3.12 TIM Timer Characteristics

Table 3-23 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80MHz$	12.5		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 80MHz$	0	40	MHz
R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80MHz$	0.0125	819	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 80MHz$		53.7	s

3.3.13 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram

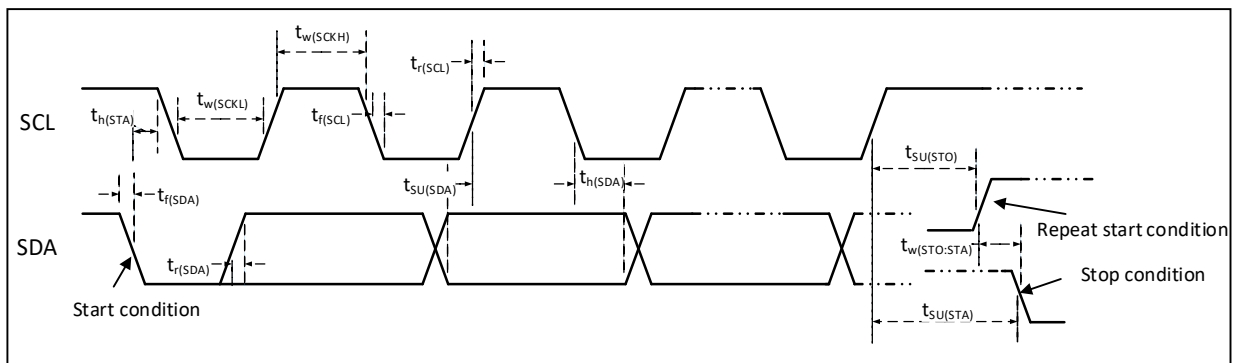


Table 3-24 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{su(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{su(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us

C_b	Capacitive load for each bus		400		400	pF
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3.3.14 I3C Interface Characteristics

Table 3-25 I3C interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{r(SDA_OD)}^{(1)}$	SDA rise time in open-drain mode		100		ns
$t_{r(SDA_PP)}^{(1)}$	SDA rise time in push-pull mode		5.1		ns

Note: 1. $t_{r(SDA_OD)}$ and $t_{r(SDA_PP)}$ are guaranteed design parameters and can be configured via register $R32_I3C_TIMINGR0$. For other timing parameters, refer to the MIPI protocol.

3.3.15 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode

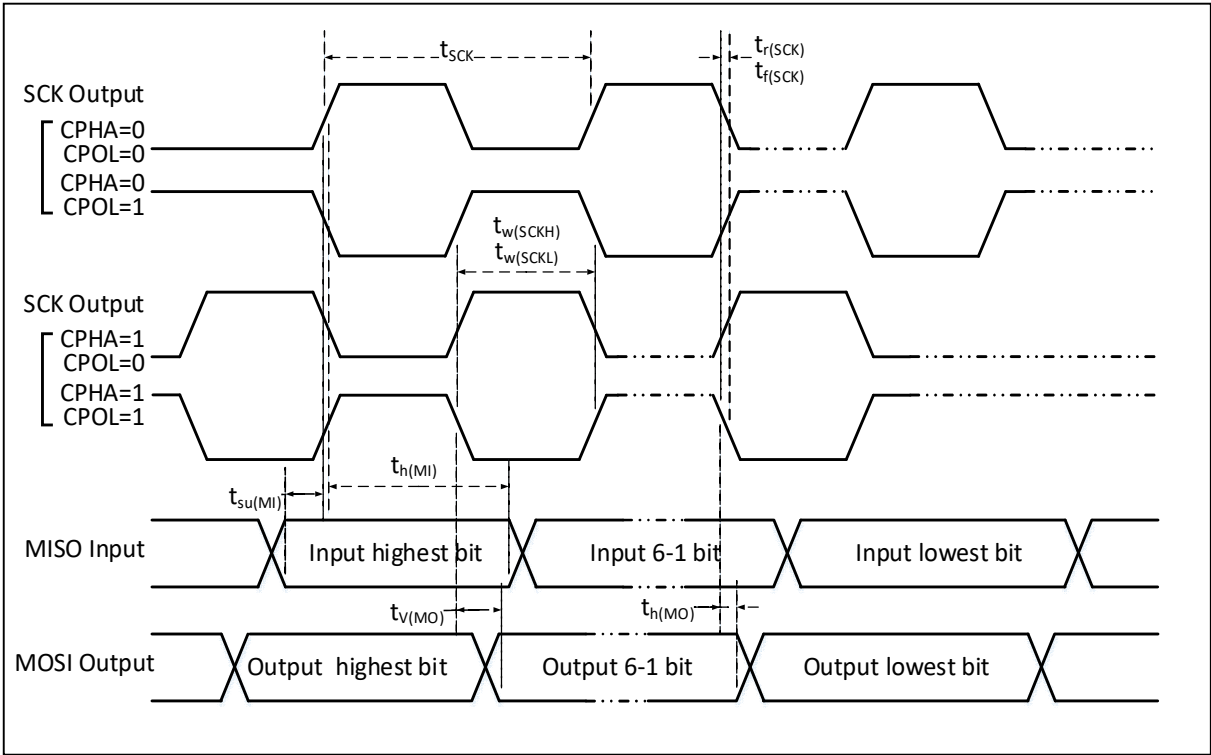


Figure 3-10 SPI timing diagram in Slave mode (CPHA=0)

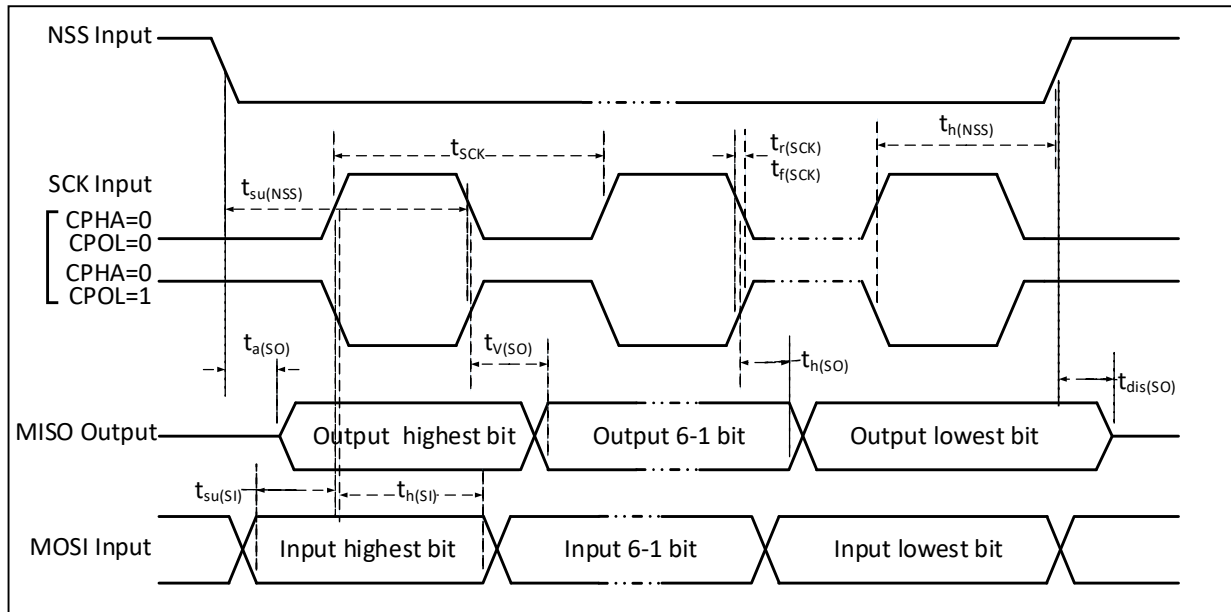


Figure 3-11 SPI timing diagram in Slave mode (CPHA=1)

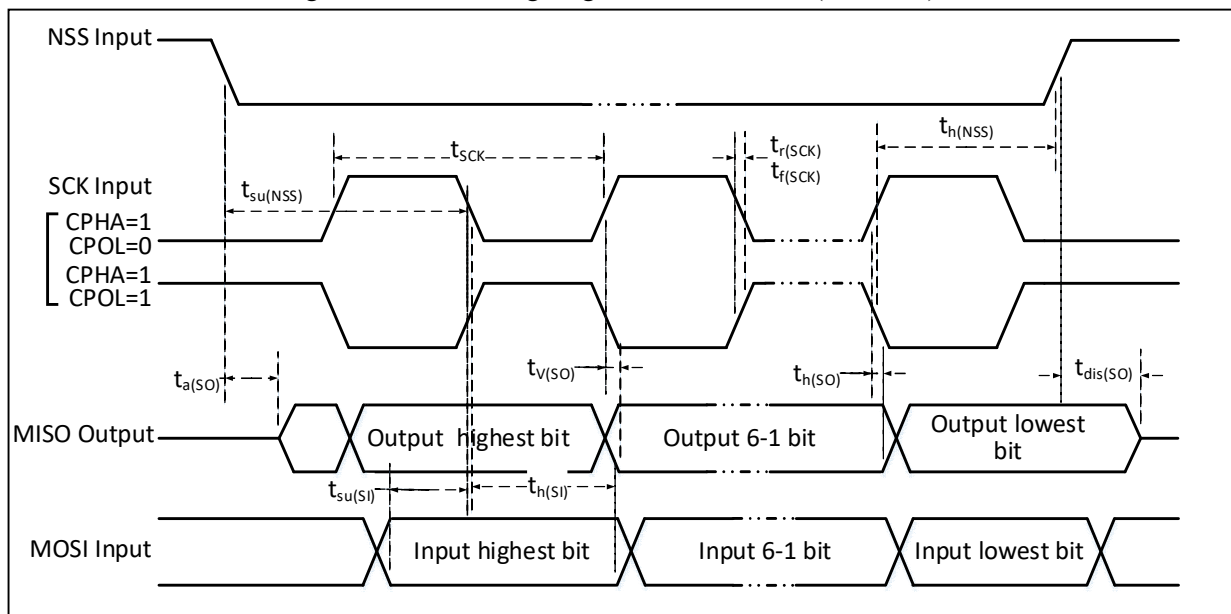


Table 3-26 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		80	MHz
		Slave mode		80	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2 \cdot t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2 \cdot t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, $f_{PCLK} = 24MHz$, Prescaler factor = 4	70	97	ns

$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	10	ns
		Master mode	HSRXEN = 1	$10-0.5*t_{SC}$ K	
$t_{SU(SI)}$		Slave mode		4	ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4	ns
		Master mode	HSRXEN = 1	$0.5*t_{SCK}-4$	
$t_{h(SI)}$		Slave mode		4	ns
$t_{a(SO)}$	Data output access time	Slave mode, $f_{HCLK} = 20MHz$		0	$1*t_{HCLK}$ ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10 ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			10 ns
$t_{V(MO)}$		Master mode (After enable edge)			5 ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)		8	ns
$t_{h(MO)}$		Master mode (After enable edge)		0	ns

3.3.16 I2S Interface Characteristics

Figure 3-12 I2S Bus master mode timing diagram

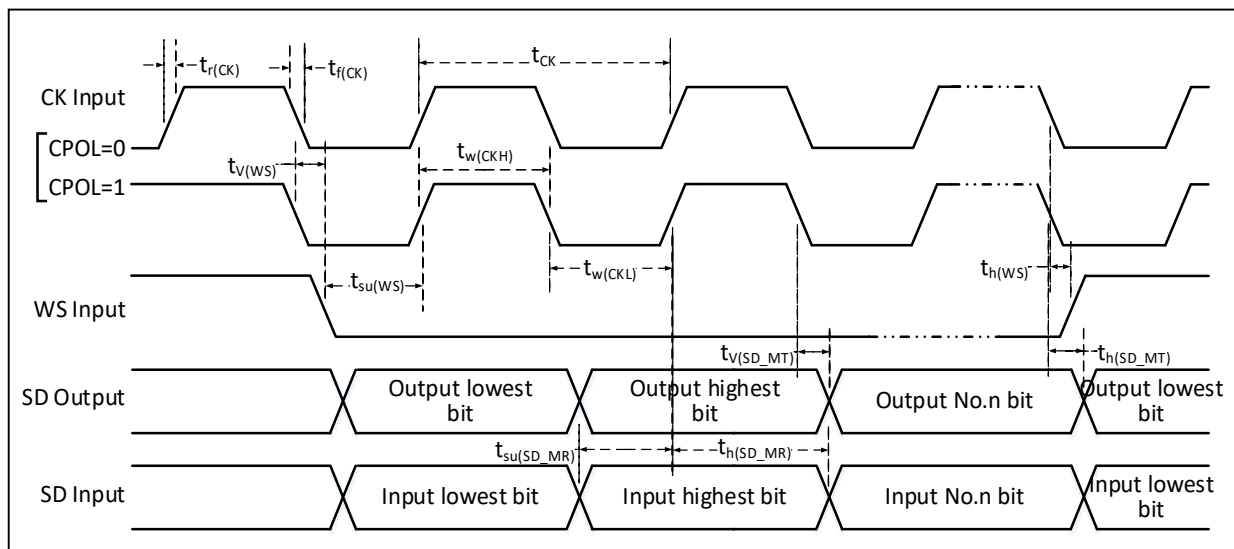


Figure 3-13 I2S Bus slave mode timing diagram

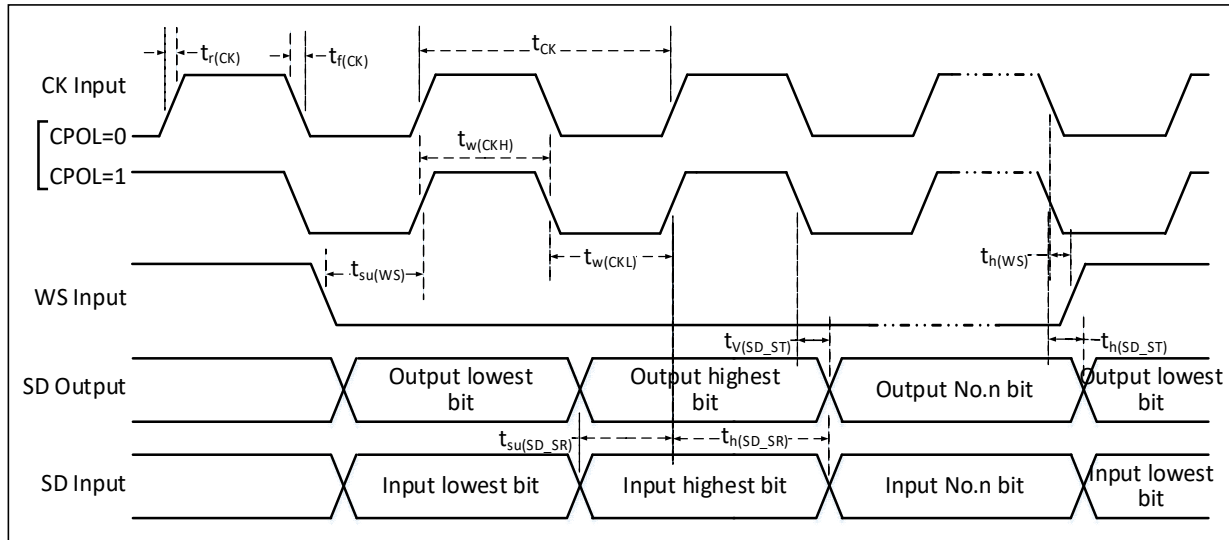


Table 3-27 I2S interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{CK}/t_{CK}	I2S clock frequency	Master mode		8	MHz
		Slave mode		8	MHz
$t_{r(CK)}/t_{f(CK)}$	I2S clock rise and fall time	Load capacitance: C = 30pF		20	ns
$t_{v(WS)}$	WS valid time	Master mode		5	ns
$t_{su(WS)}$	WS setup time	Slave mode	10		ns
$t_{h(WS)}$	WS hold time	Master mode	0		ns
		Slave mode	0		ns
$t_{w(CKH)}/t_{w(CKL)}$	SCK high level and low level time	Master mode, $f_{HCLK} = 36\text{MHz}$ prescaler factor = 4	40	60	%
$t_{su(SD_MR)}/t_{su(SD_SR)}$	Data input setup time	Master mode	8		ns
		Slave mode	8		ns
$t_{h(SD_MR)}/t_{h(SD_SR)}$	Data input hold time	Master mode	5		ns
		Slave mode	4		ns
$t_{h(SD_MT)}$	Data output hold time	Slave mode (After enabling edge)		5	ns
$t_{h(SD_ST)}$		Master mode (After enabling edge)		5	ns
$t_{v(SD_MT)}$		Slave mode (After enabling edge)		5	ns
$t_{v(SD_ST)}$	Data output valid time	Master mode (After enabling edge)		4	ns

3.3.17 USB 2.0 Interface Characteristics

Table 3-28 USB 2.0 interface I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	USB 2.0 operating voltage		3.15		3.45	V
V_{SE}	Single ended receiver	$V_{DD33} = 3.3\text{V}$	1.2		1.9	V

	threshold					
V_{OL}	Static output low level				0.3	V
V_{OH}	Static output high level		2.8		V_{DD}	V
V_{HSSQ}	Detection threshold of high-speed pressing information		100		150	mV
V_{HSDSC}	Detection threshold of high-speed disconnection		500		625	mV
V_{HSOI}	High-speed idle level		-10		10	mV
V_{HSOH}	High-speed data high level		360		440	mV
V_{HSOL}	High-speed data low level		-10		10	mV
R_{USBPU}	USB pin pull-up resistor		1.3	1.5	1.8	k Ω
R_{USBPD}	USB pin pull-down resistor		13	15	18	k Ω
V_{BC_REF}	BC CMP reference voltage			0.4		V
V_{BC_SRC}	BC protocol output voltage			0.6		V

3.3.18 SDIO Interface Characteristics

Table 3-29 SDIO interface I/O characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit	
f_{CK}/t_{CK}	Clock frequency in data transmission mode	CL≤10pF, 4-wire mode and mapping to HS pin		80	MHz	
		CL≤30pF, 4-wire or 8-wire mode		50		
$t_{W(CKL)}$	Clock low level time	CL≤30pF	3		ns	
$t_{W(CKH)}$	Clock high level time	CL≤30pF	3			
$t_{r(CK)}$	Rising time	CL≤30pF		2		
$t_{f(CK)}$	Falling time	CL≤30pF		2		
CMD/DAT input (Refer to CK)						
t_{ISU}	Input setup time	CL≤30pF	5		ns	
t_{IH}	Input holding time	CL≤30pF	1			
In high-speed mode, CMD/DAT output (refer to CK)						
t_{OV}	Output valid time	CL≤30pF	Master mode		3	ns
			Slave mode		9	
t_{OH}	Output holding time	CL≤30pF	10			
In default mode, CMD/DAT output (refer to CK)						
t_{OVD}	Output valid default time	CL≤30pF	Master mode		4	ns
			Slave mode		10	
t_{OHD}	Output holding default time	CL≤30pF	10			

3.3.19 FSMC Characteristics

Figure 3-14 Asynchronous bus multiplexing PSRAM/NOR read operation waveform

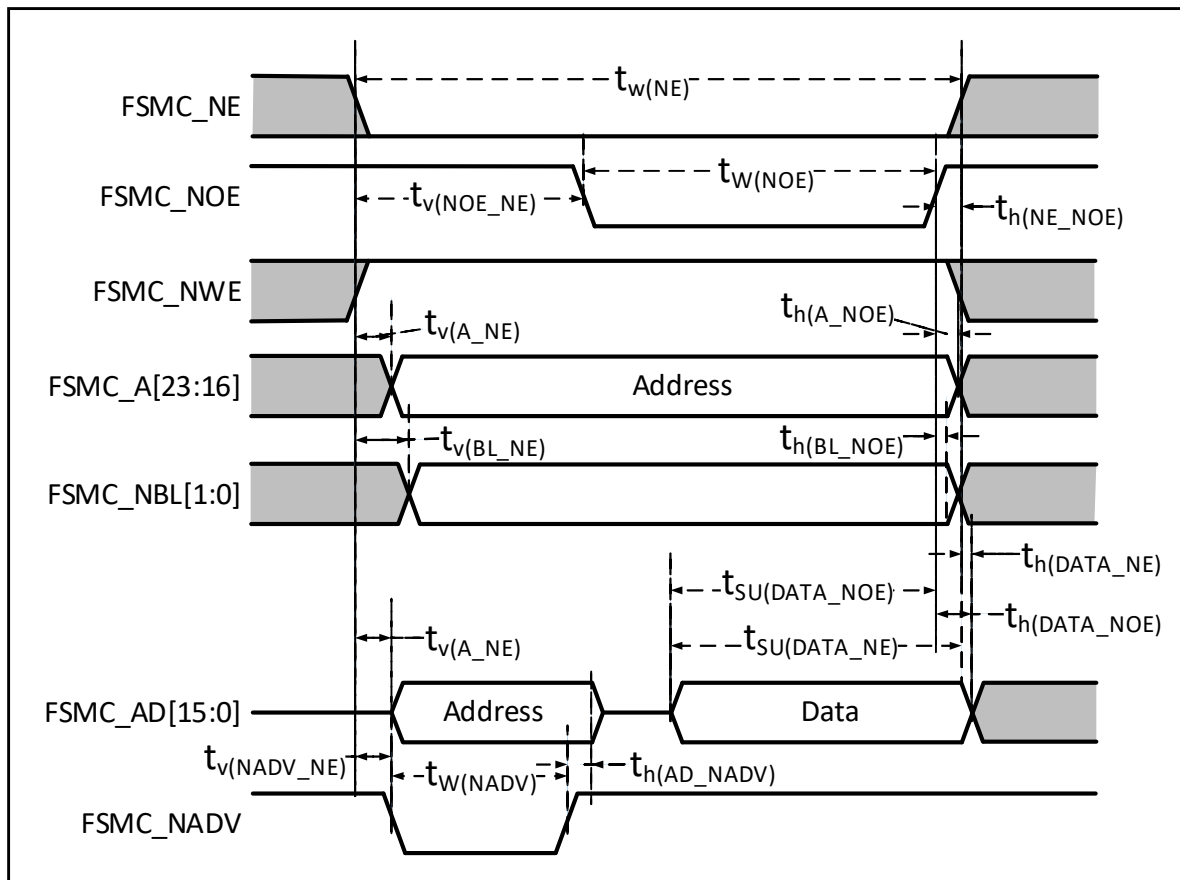


Table 3-30 Timing of PSRAM/NOR read operation for asynchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_w(NE)$	FSMC_NE low level time	$7 \cdot t_{HCLK}$		ns
$t_v(NO_NE)$	FSMC_NE low to FSMC_NOE low	0		
$t_w(NO_E)$	FSMC_NOE low time	$7 \cdot t_{HCLK}$		
$t_h(NE_NOE)$	Retention time from FSMC_NOE high to FSMC_NE high	0		
$t_v(A_NE)$	FSMC_NE low to FSMC_A active	0	5	
$t_v(NADV_NE)$	FSMC_NE low to FSMC_NADV low	0	5	
$t_w(NADV)$	FSMC_NADV low time	t_{HCLK}		
$t_h(AD_NADV)$	Effective retention time of FSMC_AD (address) after FSMC_NADV is high.	$2 \cdot t_{HCLK}$		
$t_h(A_NOE)$	Address retention time after FSMC_NOE is high	0		
$t_h(BL_NOE)$	FSMC_BL holding time after FSMC_NOE is high.	0		
$t_v(BL_NE)$	FSMC_NE low to FSMC_BL active	0	5	
$t_{SU}(DATA_NE)$	Setup time from data to FSMC_NE high	$3 \cdot t_{HCLK}$		
$t_{SU}(DATA_NOE)$	Setup time from data to FSMC_NOE high	$3 \cdot t_{HCLK}$		
$t_h(DATA_NE)$	Data retention time after FSMC_NE is high	0		
$t_h(DATA_NOE)$	Data retention time after FSMC_NOE is high	0		

Figure 3-15 Asynchronous bus multiplexing PSRAM/NOR write operation waveform

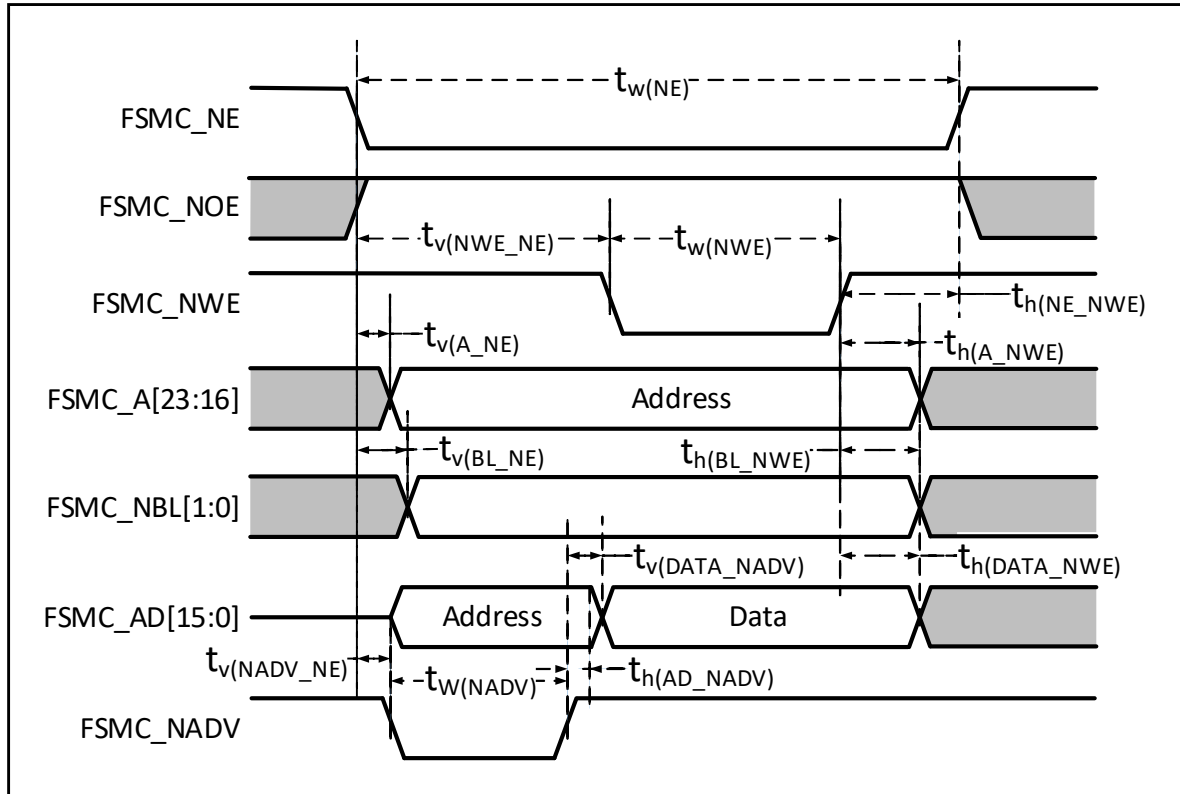


Table 3-31 Timing of PSRAM/NOR write operation for asynchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_{w(NE)}$	FSMC_NE low level time	$5 * t_{HCLK}$		ns
$t_{v(NE_NWE)}$	FSMC_NE low to FSMC_NWE low	$3 * t_{HCLK}$		
$t_{w(NWE)}$	FSMC_NWE low time	$2 * t_{HCLK}$		
$t_{h(NE_NWE)}$	Retention time from FSMC_NWE high to FSMC_NE high	t_{HCLK}		
$t_{v(A_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{v(NADV_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h(AD_NADV)}$	Effective retention time of FSMC_AD (address) after FSMC_NADV is high.	$2 * t_{HCLK}$		
$t_{h(A_NWE)}$	Address retention time after FSMC_NWE is high	t_{HCLK}		
$t_{v(BL_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{h(BL_NWE)}$	FSMC_BL retention time after FSMC_NWE is high	t_{HCLK}		
$t_{v(DATA_NADV)}$	FSMC_NADV high to data retention time	$2 * t_{HCLK}$		
$t_{h(DATA_NWE)}$	Data retention time after FSMC_NWE is high	t_{HCLK}		

Figure 3-16 Synchronous bus multiplexing NOR/PSRAM read waveform

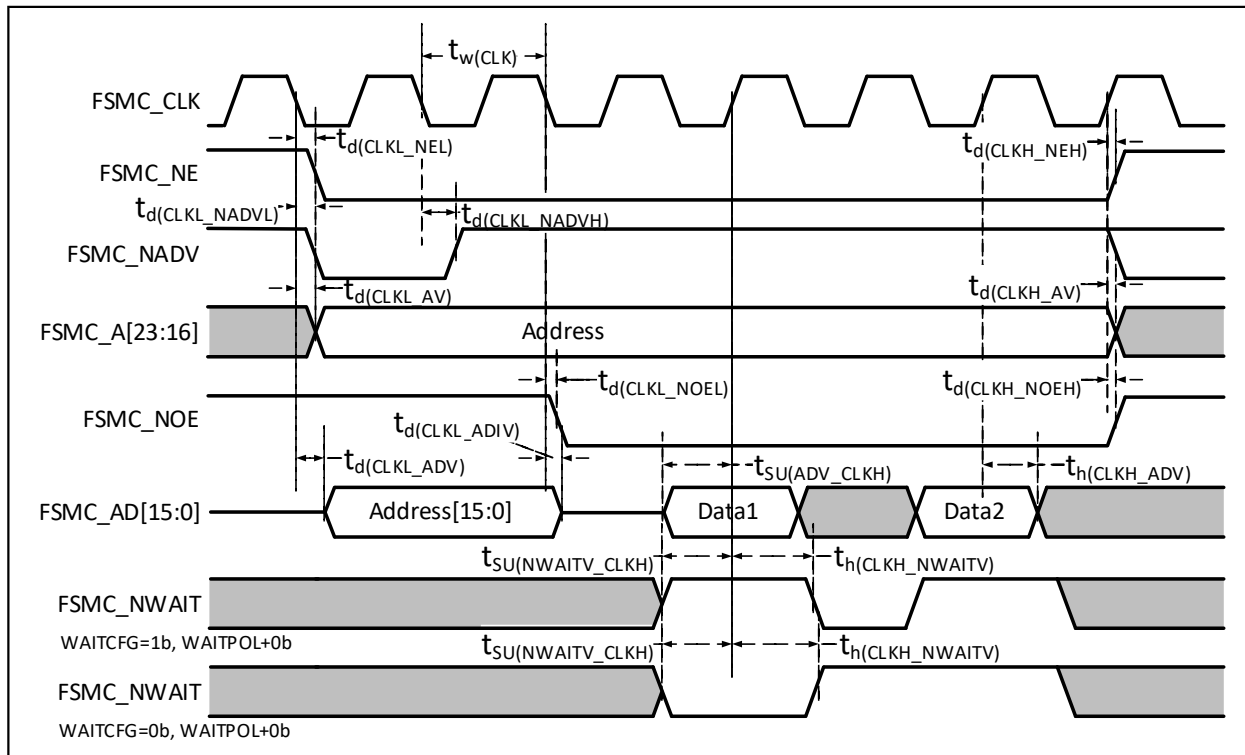


Table 3-32 Timing of NOR/PSRAM read operation for synchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_w(\text{CLK})$	FSMC_CLK cycle	$2 \cdot t_{\text{HCLK}}$		ns
$t_d(\text{CLKL_NEL})$	FSMC_CLK low to FSMC_NE low	0	5	
$t_d(\text{CLKH_NEH})$	FSMC_CLK high to FSMC_NE high	$0.5 \cdot t_{\text{HCLK}}$	$0.5 \cdot t_{\text{HCLK}}$	
$t_d(\text{CLKL_NADVL})$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_d(\text{CLKL_NADVH})$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_d(\text{CLKL_AV})$	FSMC_CLK low to FSMC_Ax valid (x = 16...23)	0	5	
$t_d(\text{CLKH_AIV})$	FSMC_CLK high to FSMC_Ax invalid (x = 16...23)	0	5	
$t_d(\text{CLKL_NOEL})$	FSMC_CLK low to FSMC_NOE low	$2 \cdot t_{\text{HCLK}}$		
$t_d(\text{CLKH_NOEH})$	FSMC_CLK high to FSMC_NOE high	t_{HCLK}		
$t_d(\text{CLKL_ADV})$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_d(\text{CLKL_ADIV})$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{\text{SU}}(\text{ADV_CLKH})$	FSMC_CLK high before FSMC_AD[15:0] valid data	8		
$t_{\text{h}}(\text{CLKH_ADV})$	FSMC_CLK high after FSMC_AD[15:0] valid data	8		
$t_{\text{SU}}(\text{NWAITV_CLKH})$	FSMC_CLK high before FSMC_NWAIT valid	6		
$t_{\text{h}}(\text{CLKH_NWAITV})$	FSMC_CLK high after FSMC_NWAIT valid	2		

Figure 3-17 Synchronous bus multiplexing PSRAM write waveform

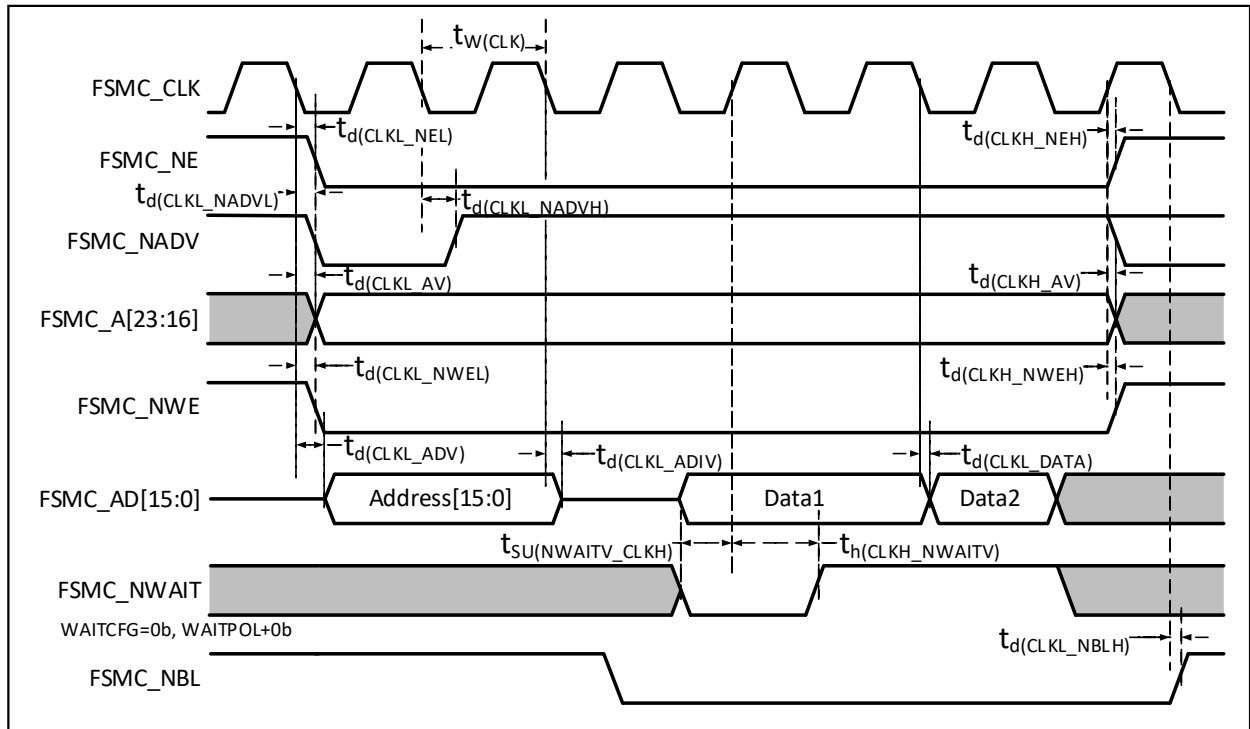


Table 3-33 Timing of NOR/PSRAM read operation for synchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_W(\text{CLK})$	FSMC_CLK cycle	$2 \cdot t_{HCLK}$		
$t_d(\text{CLK}_L_NEL)$	FSMC_CLK low to FSMC_NE low	0	5	ns
$t_d(\text{CLK}_H_NEH)$	FSMC_CLK high to FSMC_NE high	$0.5 \cdot t_{HCLK}$	$0.5 \cdot t_{HCLK}$	
$t_d(\text{CLK}_L_NADV_L)$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_d(\text{CLK}_L_NADV_H)$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_d(\text{CLK}_L_AV)$	FSMC_CLK low to FSMC_Ax valid (x = 16...23)	0	5	
$t_d(\text{CLK}_H_AIV)$	FSMC_CLK high to FSMC_Ax invalid (x = 16...23)	0	5	
$t_d(\text{CLK}_L_NWE_L)$	FSMC_CLK low to FSMC_NWE low	0		
$t_d(\text{CLK}_H_NWEH)$	FSMC_CLK high to FSMC_NWE high	0		
$t_d(\text{CLK}_L_ADV)$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_d(\text{CLK}_L_ADIV)$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_d(\text{CLK}_L_DATA)$	FSMC_CLK low after FSMC_AD[15:0] valid	2		
$t_{SU}(\text{NWAITV_CLKH})$	FSMC_CLK high before FSMC_NWAIT valid	6		
$t_h(\text{CLKH_NWAITV})$	FSMC_CLK high after FSMC_NWAIT valid	2		
$t_d(\text{CLK}_L_NBLH)$	FSMC_CLK low to FSMC_NBL high	2		

Waveform and timing of NAND controller

Test conditions: NAND operation mode, 16-bit data width selected, ECC calculation circuit enabled, 512-byte page size. Other timing configurations set via configuration registers: FSMC_PCR2=0x0002005E, FSMC_PMEM2=0x01020301, FSMC_PATT2=0x01020301.

Figure 3-18 NAND controller read operation waveform

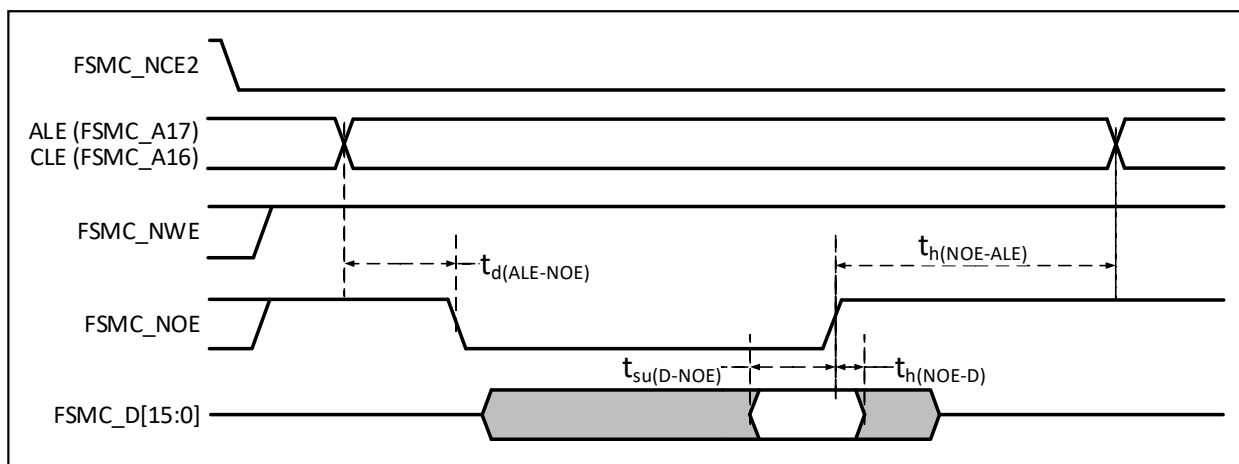


Figure 3-19 NAND controller write operation waveform

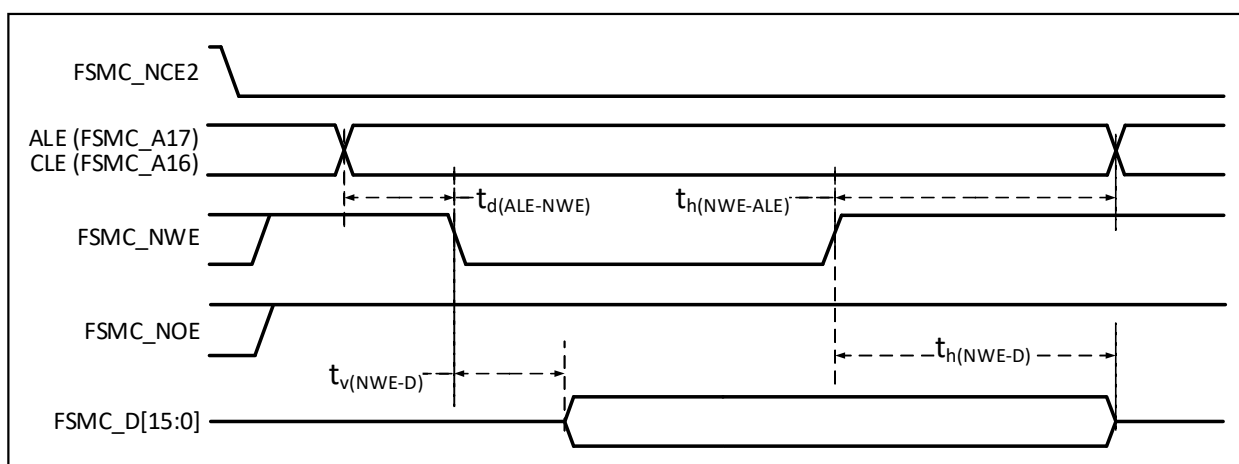


Figure 3-20 Read operation waveform of NAND controller in general storage space

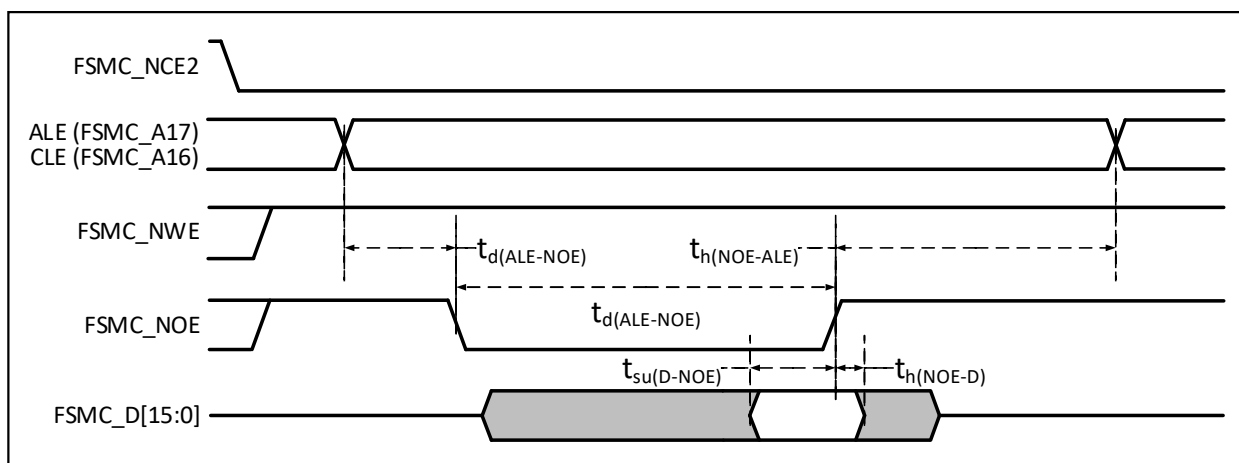


Figure 3-21 Write operation waveform of NAND controller in general storage space

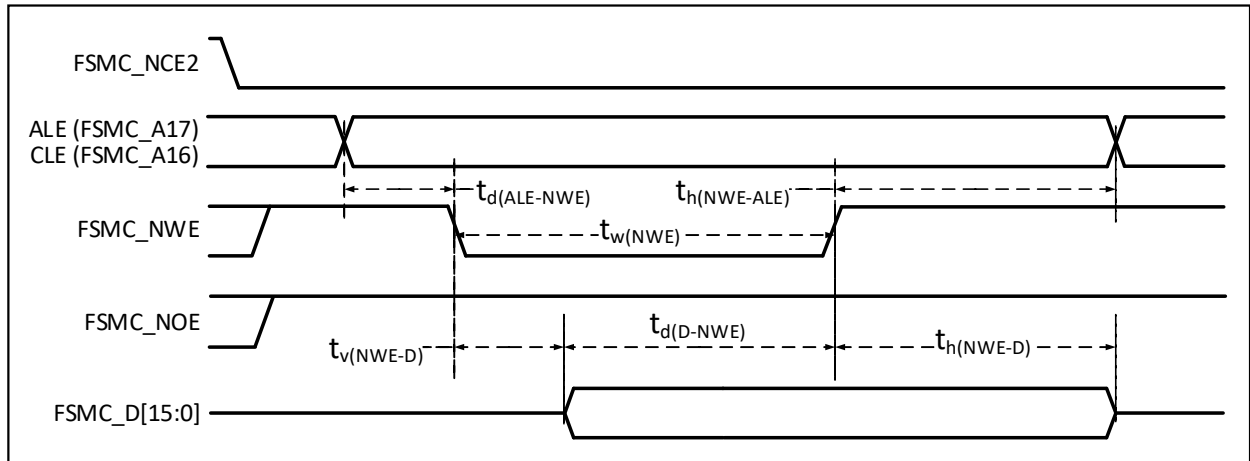


Table 3-34 Timing characteristics of read/write cycle of NAND Flash memory

Symbol	Parameter	Min.	Max.	Unit
t_d (D-NWE)	FSMC_NWE high before FSMC_D[15:0] data is valid	$4 \cdot t_{HCLK}$		ns
t_w (NOE)	FSMC_NOE low time	$4 \cdot t_{HCLK}$		
t_{su} (D-NOE)	FSMC_NOE high before FSMC_D[15:0] data is valid	20		
t_h (NOE-D)	FSMC_NOE high after FSMC_D[15:0] data is valid	15		
t_w (NWE)	FSMC_NWE low time	$4 \cdot t_{HCLK}$		
t_v (NWE-D)	FSMC_NWE low to FSMC_D[15:0] data valid	0		
t_h (NWE-D)	FSMC_NWE high to FSMC_D[15:0] data invalid	$2 \cdot t_{HCLK}$		
t_d (ALE-NWE)	FSMC_NWE low before FSMC_ALE valid	$2 \cdot t_{HCLK}$		
t_h (NWE-ALE)	FSMC_NWE high to FSMC_ALE invalid	$2 \cdot t_{HCLK}$		
t_d (ALE-NOE)	FSMC_NOE low before FSMC_ALE valid	$2 \cdot t_{HCLK}$		
t_h (NOE-ALE)	FSMC_NOE high to FSMC_ALE invalid	$4 \cdot t_{HCLK}$		

3.3.20 DVP Interface Characteristics

Figure 3-22 DVP timing waveform

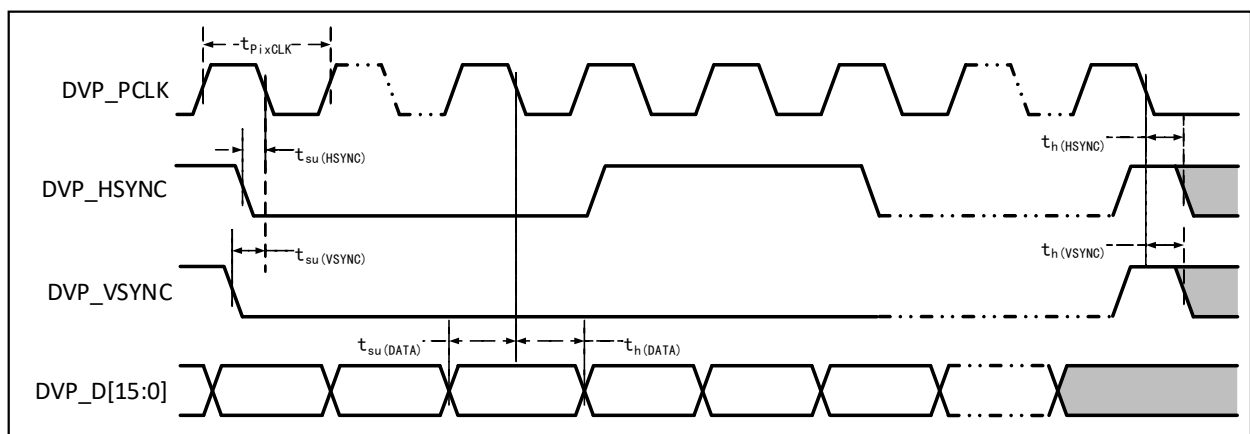


Table 3-35 DVP interface characteristics

Symbol	Parameter	Min.	Max.	Unit
$f_{\text{PixCLK}}/t_{\text{PixCLK}}$	Pixel clock input frequency		150	MHz
Duty(PixCLK)	Duty cycle of pixel clock	15		%
$t_{\text{su}}(\text{DATA})$	Data setup time	2.5		ns
$t_{\text{h}}(\text{DATA})$	Data holding time	1		ns
$t_{\text{su}}(\text{HSYNC})/t_{\text{su}}(\text{VSYNC})$	DVP_HSYNC/DVP_VSYNC signal input setup time	2.5		ns
$t_{\text{h}}(\text{HSYNC})/t_{\text{h}}(\text{VSYNC})$	DVP_HSYNC/DVP_VSYNC signal input holding time	1		ns

3.3.21 12-bit ADC Characteristics

Table 3-36 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.9		3.6	V
$V_{\text{REF+}}^{(2)(3)}$	Positive reference voltage	$V_{\text{REF+}} \leq V_{\text{DDA}}$	2.4		V_{DDA}	V
I_{DDA}	V_{DDA} supply current			1		uA
I_{REFP}	$V_{\text{REF+}}$ supply current			30		uA
f_{ADC}	ADC clock frequency				30	MHz
f_{s}	Sampling rate				2	MHz
V_{AIN}	Conversion voltage range		0		$V_{\text{REF+}}$	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.2		kΩ
C_{ADC}	Internal sample and hold capacitor			8		pF
t_{CAL}	Calibration time			136		1/ f_{ADC}
t_{lat}	Injected trigger conversion latency				2	1/ f_{ADC}
t_{latr}	Regular trigger conversion latency				2	1/ f_{ADC}
t_{s}	Power-on time		1.5		239.5	1/ f_{ADC}
t_{CONV}	Total conversion time (including sampling time)		14		252	1/ f_{ADC}

Note: All above are design parameters.

Formula 1: Maximum R_{AIN}

$$R_{\text{AIN}} \leq \frac{T_{\text{s}}}{f_{\text{ADC}} \times C_{\text{ADC}} \times \ln 2^{N+1}} - R_{\text{ADC}}$$

The above Formula 1 is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 3-37 Maximum R_{AIN} when $f_{\text{ADC}} = 30\text{MHz}$

$T_{\text{s}}(\text{cycle})$	$t_{\text{s}}(\text{us})$	Maximum $R_{\text{AIN}}(\text{k}\Omega)$
2.5	0.08	0.87
5.5	0.18	2.16
7.5	0.25	3.02

11.5	0.38	4.73
13.5	0.45	5.59
28.5	0.95	12.03
41.5	1.38	17.61
239.5	7.98	50

Table 3-38 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
E0	Offset error	$f_{\text{ADC}} = 30\text{MHz}$, $R_{\text{AIN}} < 2\text{k}\Omega$, $V_{\text{DDA}} = 3.3\text{V}$		± 3	± 6	LSB
ED	Differential nonlinearity error			± 3	± 5	
EL	Integral nonlinearity error			± 3	± 6	

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-23 ADC typical connection diagram

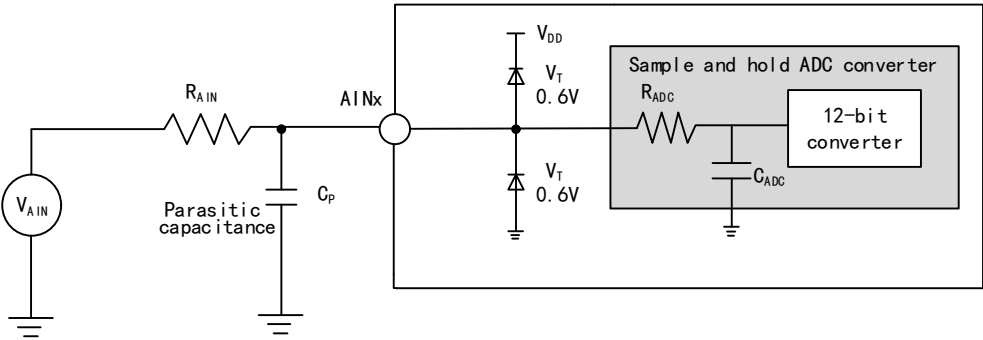
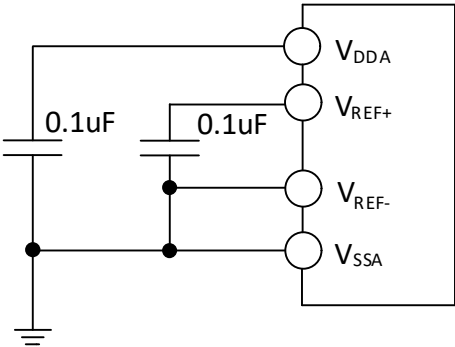


Figure 3-24 Analog power supply and decoupling circuit reference



3.3.22 Temperature Sensor Characteristics

Table 3-39 Temperature sensor characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R _{TS}	Measurement range of temperature		-40		85	°C

	sensor					
A _{TSC}	Measurement range of temperature sensor after software calibration			±12		°C
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.8	mV/°C
V ₂₅	Voltage at 25°C		1.34	1.40	1.46	V
T _{S_temp}	ADC sampling time when reading temperature	f _{ADC} = 14MHz			17.1	us

3.3.23 DAC Characteristics

Table 3-40 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DDA}	Supply voltage		2.9	3.3	3.6	V
V _{REF+}	Positive reference voltage	V _{REF+} ≤ V _{DDA}	2.4	3.3	3.6	V
R _L ⁽¹⁾	Load resistance when the buffer is open		5			kΩ
	Load resistance when the buffer is closed		15			kΩ
C _L ⁽¹⁾	Load capacitance when buffer is open				50	pF
V _{OUT_MIN} ⁽¹⁾	Buffer on, 12-bit DAC conversion		0		8	mV
V _{OUT_MAX} ⁽¹⁾		V _{REFP} = 3.3V	3.29		3.3	V
V _{OUT_MIN} ⁽¹⁾	Buffer off, 12-bit DAC conversion		0		3	mV
V _{OUT_MAX} ⁽¹⁾		V _{REFP} = 3.3V	3.295		3.3	V
I _{VREFP}	No load, input value 0x800			58		uA
	No load, when V _{REFP} = 3.6V, the input value is 0xF1C			194		
	No load, when V _{REFP} = 3.6V, the input value is 0x555 (worst)			331		
I _{DDA}	Buffer opened without load, input value 0x800			170		uA
	Buffer open without load, V _{REFP} = 3.6V, input value 0xF1C			150		
	Buffer open without load, V _{REFP} = 3.6V, input value 0x555 (worst)			170		
DNL	Differential nonlinear error			±2		LSB
INL	Integral nonlinear error	After offset error and gain error correction		±4		LSB
Lose balance	Offset error			±3	±12	mV
		V _{REFP} = 3.6V			±10	LSB
Gain error		DAC configured as 12-bit		±0.4		%
Amplifier gain ⁽¹⁾	Amplifier gain with open loop	5kΩ load (max.)	80	85		dB
t _{SETTLING}	The maximum frequency of the correct DAC_OUT is obtained when the input code is a small change (from the value i to i+1 LSB)	C _{LOAD} ≤ 50pF R _{LOAD} ≥ 5kΩ		3	4	us
Update rate	When the input code changes slightly	C _{LOAD} ≤ 50pF			1	MS/s

	(from the value I to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained.	$R_{LOAD} \geq 5k\Omega$				
t_{WAKEUP}	Time to wake up from sleep mode (when the DAC enable bit ENx changes from 0 to 1)	$C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$, input code is between the minimum and maximum possible values		6.5	10	us
$PSRR^{+ (1)}$	Power supply rejection ratio (relative to V_{DD33A}) (static DC measurement)	Without R_{LOAD} , $C_{LOAD} \leq 50pF$		-100	-75	dB

Note: 1. Design parameters are guaranteed.

3.3.24 OPA Characteristics

Table 3-41-1 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.9	3.3	3.6	V
V_{CMIR}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage			± 2.5	± 10	mV
I_{LOAD}	Drive current				600	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		195		uA
$C_{MRR}^{(1)}$	Common mode rejection ratio	@1kHz		96		dB
$P_{SRR}^{(1)}$	Power supply rejection ratio	@1kHz		86		dB
$A_V^{(1)}$	Open loop gain	$C_{LOAD} = 5pF$		136		dB
$G_{BW}^{(1)}$	Unit gain bandwidth	$C_{LOAD} = 5pF$		19		MHz
$P_M^{(1)}$	Phase margin	$C_{LOAD} = 5pF$		93		°
$S_R^{(1)}$	Slew rate limited	$C_{LOAD} = 5pF$		8		V/us
$t_{WAKUP}^{(1)}$	Setup time from shutdown to wake up, 0.1%	Input $V_{DDA}/2$, $C_{LOAD} = 50pF$, $R_{LOAD} = 4k\Omega$			0.5	us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
$V_{OHSAT}^{(2)}$	High saturation output voltage	$R_{LOAD} = 4k\Omega$, input V_{DDA}	$V_{DDA}-300$	$V_{DDA}-150$		mV
		$R_{LOAD} = 20k\Omega$, input V_{DDA}	$V_{DDA}-50$	$V_{DDA}-30$		mV
$V_{OLSAT}^{(2)}$	Low saturation output voltage	$R_{LOAD} = 4k\Omega$, input 0		3	10	mV
		$R_{LOAD} = 20k\Omega$, input 0		3	10	mV
PGA Gain ⁽¹⁾	PGADIF = 0, in-phase PGA gain error	Gain = 4, $V_{CMIR} < (V_{DDA}/3)$	-1		1	%
		Gain = 8, $V_{CMIR} < (V_{DDA}/7)$	-1		1	%
		Gain = 16, $V_{CMIR} < (V_{DDA}/15)$	-1		1	%

	PGADIF = 1, in-phase PGA gain error	Gain = 32, $V_{CMIR} < (V_{DDA}/31)$	-1.5		1.5	%
		Gain = 4	-2		2	%
		Gain = 8	-2		2	%
		Gain = 16	-2		2	%
		Gain = 32	-2.5		2.5	%
Delta R	Absolute value change of resistance		-15		15	%
EN ⁽¹⁾	Equivalent input noise	$R_{LOAD} = 4k\Omega @ 1kHz$		100		nV/ sqrt(Hz)
		$R_{LOAD} = 20k\Omega @ 1KHz$		60		

Note:

1. Design parameters;

2. Load current will limit the saturated output voltage;

Table 3-41-2 OPA characteristics (High-speed mode)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.9	3.3	3.6	V
V_{CMIR}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage			± 2.5	± 10	mV
I_{LOAD}	Drive current				600	μA
$I_{DDOPAMP}$	Current consumption	No load, static mode		770		μA
$C_{MRR}^{(1)}$	Common mode rejection ratio	@1kHz		96		dB
$P_{SRR}^{(1)}$	Power supply rejection ratio	@1kHz		86		dB
$A_V^{(1)}$	Open loop gain	$C_{LOAD} = 5pF$		136		dB
$G_{BW}^{(1)}$	Unit gain bandwidth	$C_{LOAD} = 5pF$		53		MHz
$P_M^{(1)}$	Phase margin	$C_{LOAD} = 5pF$		93		°
$S_R^{(1)}$	Slew rate limited	$C_{LOAD} = 5pF$		16		V/us
$t_{WAKUP}^{(1)}$	Setup time from shutdown to wake up, 0.1%	Input $V_{DDA}/2$, $C_{LOAD} = 50pF$, $R_{LOAD} = 4k\Omega$			0.5	μs
R_{LOAD}	Resistive load		4			$k\Omega$
C_{LOAD}	Capacitive load				30	pF
$V_{OHSAT}^{(2)}$	High saturation output voltage	$R_{LOAD} = 4k\Omega$, input V_{DDA}	$V_{DDA}-300$	$V_{DDA}-150$		mV
		$R_{LOAD} = 20k\Omega$, input V_{DDA}	$V_{DDA}-50$	$V_{DDA}-30$		mV
$V_{OLSAT}^{(2)}$	Low saturation output voltage	$R_{LOAD} = 4k\Omega$, input 0		3	10	mV
		$R_{LOAD} = 20k\Omega$, input 0		3	10	mV
PGA Gain ⁽¹⁾	PGADIF = 0, in-phase PGA gain error	Gain = 4, $V_{CMIR} < (V_{DDA}/3)$	-1		1	%
		Gain = 8, $V_{CMIR} < (V_{DDA}/7)$	-1		1	%
		Gain = 16, $V_{CMIR} < (V_{DDA}/15)$	-1		1	%
		Gain = 32, $V_{CMIR} < (V_{DDA}/31)$	-1.5		1.5	%

	PGADIF = 1, in-phase PGA gain error	(V _{DDA} /31)				
		Gain = 4	-2		2	%
		Gain = 8	-2		2	%
		Gain = 16	-2		2	%
Delta R	Absolute value change of resistance	Gain = 32	-2.5		2.5	%
			-15		15	%
EN ⁽¹⁾	Equivalent input noise	R _{LOAD} = 4kΩ@1kHz		100		nV/ sqrt(Hz)
		R _{LOAD} = 20kΩ@1KHz		60		

Note:

1. Design parameters;
2. Load current will limit the saturated output voltage;

3.3.25 On-chip PSRAM Characteristics (Only for CH32V467 chip)

Table 3-42 On-chip PSRAM characteristics (Only for CH32V467 chip)

Symbo l	Parameter	Condition										Un it
		175MHz		200MHz		225MHz ⁽¹⁾		250MHz ⁽¹⁾		300MHz ⁽¹⁾		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{SYCLK}	System clock cycle	6		5		4.4		4		3.3		ns
t _{CEM}	In non-sleep mode, PSRAM_CE_n has low pulse width (CELPW[11:0]).		4		4		4		4		4	us
		3		3		3		3		3		t _{CLK}
t _{RC}	PSRAM read-write cycle (TRC[7:0])	60		60		60		60		60		ns
t _{HS}	Minimum duration of PSRAM semi-sleep mode	150		150		150		150		150		us
t _{XHS}	Time for PSRAM to exit from semi-sleep mode	150		150		150		150		150		us
t _{XPHS}	Low pulse width of PSRAM_CE_n (TXLPD[7:0]) when exiting the semi-sleep mode	60	2000	60	2000	60	2000	60	2000	60	2000	ns
t _{DPD}	Minimum duration of PSRAM deep sleep mode	500		500		500		500		500		us
t _{DPDp}	Minimum period of PSRAM deep sleep mode	500		500		500		500		500		us
t _{XDPD}	Time when PSRAM exits deep sleep mode	150		150		150		150		150		us
t _{XDPDPD}	Low pulse width of PSRAM_CE_n (TXLPD[7:0]) when exiting the deep sleep	60		60		60		60		60		ns

mode												
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Note: 1. Only for CH32V467 chips w with the fifth last digit of the lot number is not 0, PSRAM can support clocks exceeding 200MHz, support variable and instruction access, and support byte writing; and in stop mode (the voltage regulator is in low-power mode), data can be maintained.

Figure 3-25 PSRAM timing diagram (exit from semi-sleep mode)

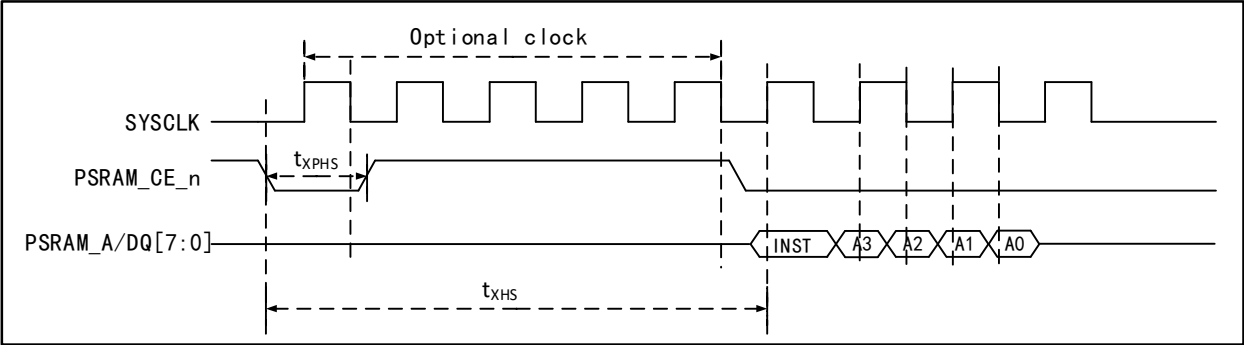
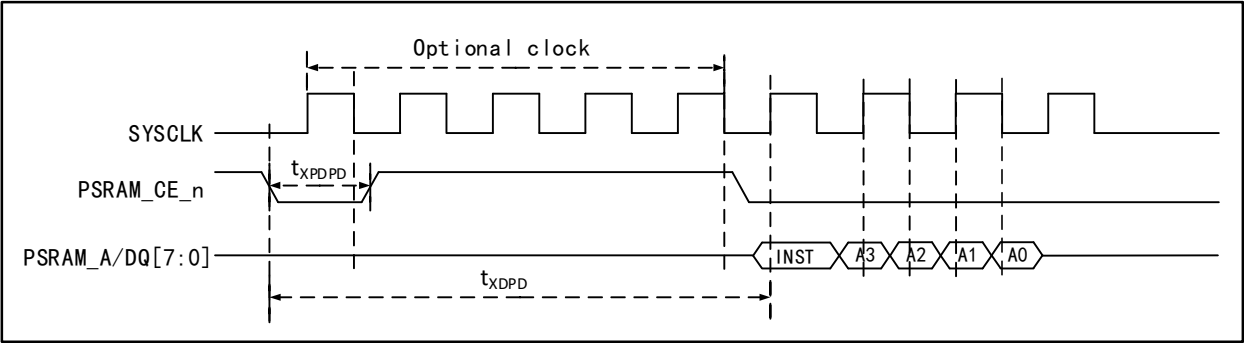


Figure 3-26 PSRAM timing diagram (exit from deep sleep mode)



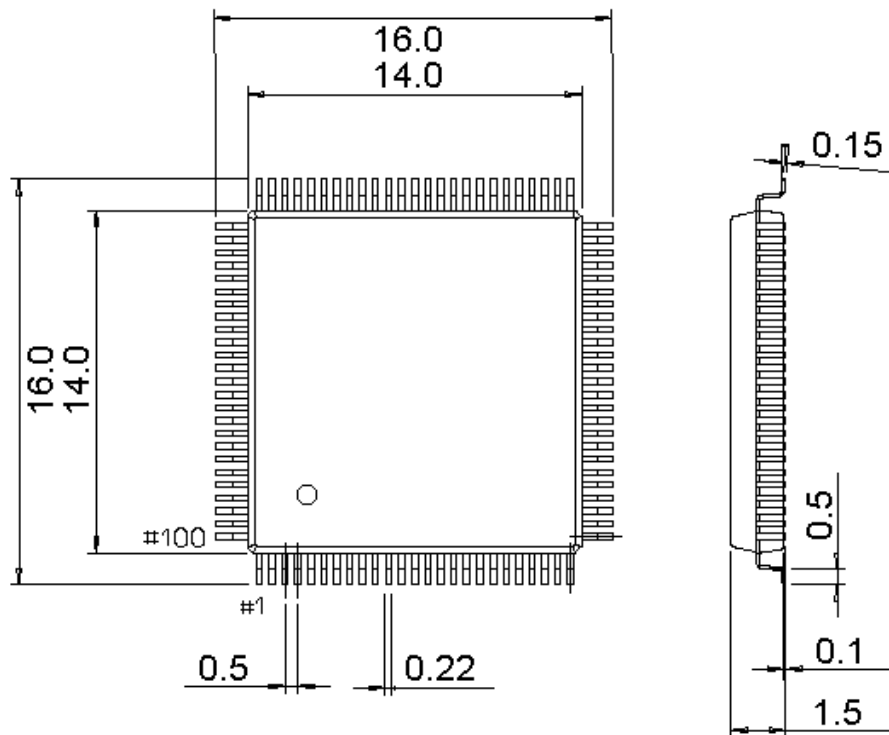
Chapter 4 Package and Ordering Information

Packages

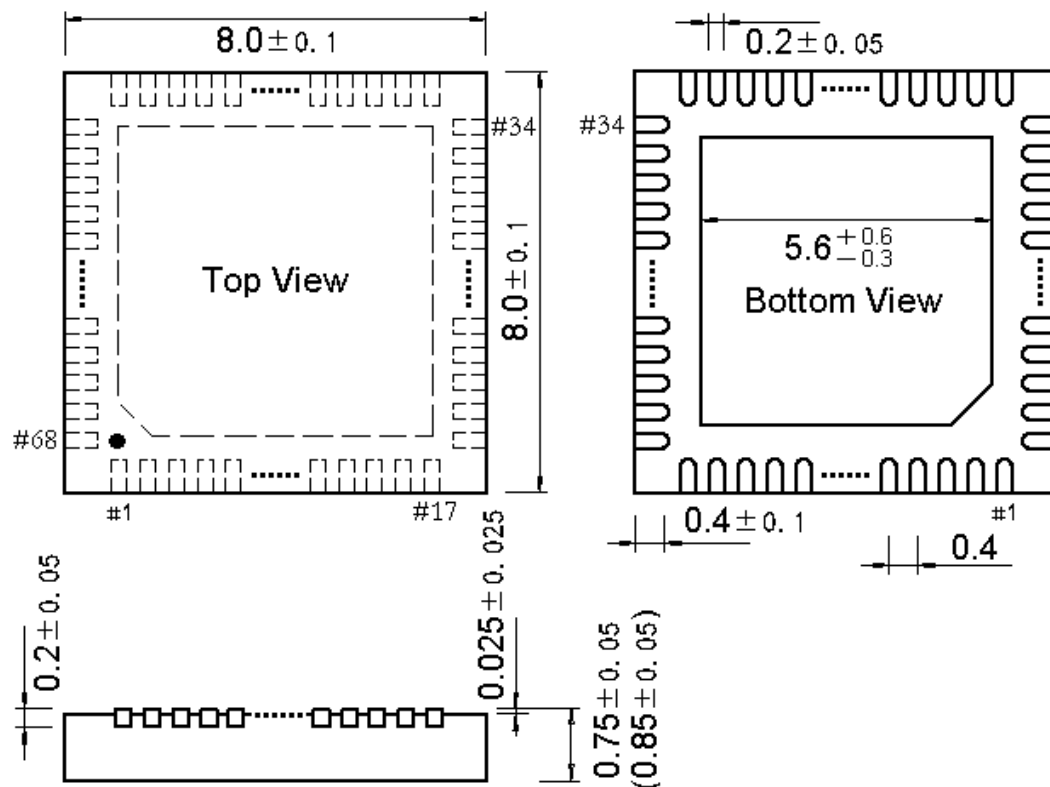
Package Form	Body size	Pin Pitch		Package Description	Order Model
LQFP100	14*14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V407VET6
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32V407WEU6
LQFP64	7*7mm	0.4mm	15.7mil	Low Profile Quad Flat Pack	CH32V407RET6
LQFP100	14*14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V467VET6
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32V467WEU6
LQFP64	7*7mm	0.4mm	15.7mil	Low Profile Quad Flat Pack	CH32V467RET6

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of $\pm 0.2\text{mm}$ or $\pm 10\%$.

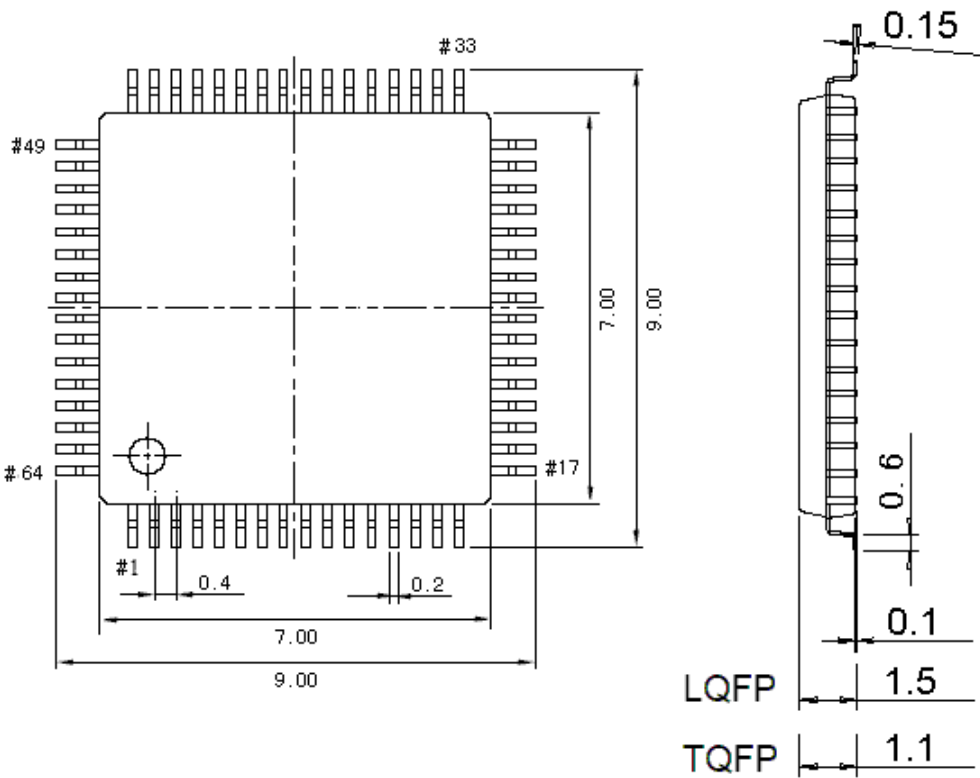
4.1 LQFP100 Package



4.2 QFN68 Package



4.3 LQFP64 Package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Product Series

F = Arm core, general-purpose MCU

V = QingKe RISC-V core, general-purpose MCU

L = QingKe RISC-V core, low-power MCU

X = QingKe RISC-V core, dedicated or special peripheral MCU

M = QingKe RISC-V core, Built-in gate drive motor MCU

H = QingKe RISC-V core, high-performance MCU

Product type (*)+Product sub-series (**)

Product type	Product sub-series
0 = Value version, main frequency <=48M	02 = 16K Flash value general-purpose type 03 = 16K Flash basic general-purpose type, OPA 06 = 64K Flash multi-function general-purpose type, OPA, dual-purpose, TKey 07 = Basic motor application type, OPA+CMP
1 = Basic version, main frequency <=100M 2 = Enhanced version, main frequency <=200M 3 = Hardware floating point, medium and large capacity <512KB	03 = Connected, USB 05 = Connected, USB HS, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (Built-in PHY), SDIO
4 = Large capacity >=512KB	17 = Interconnected, USB SS, SerDes, HSADC, UHSIF, SDIO, DVP, Ethernet (Built-in PHY)

Pin number

J = 8 pin D = 12 pin A = 16 pin F = 20 pin E = 24 pin
G = 28 pin K = 32 pin T = 36 pin C = 48 pin R = 64 pin
W = 68 pin M = 88 pin V = 100 pin Q = 128 pin Z = 144 pin

Flash memory capacity

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory 8 = 64K Flash memory
B = 128K Flash memory C = 256K Flash memory E = 512K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40°C~85°C 7 = -40°C~105°C
3 = -40°C~125°C D = -40°C~150°C