CH32V205/CH32V203 Datasheet

V1.3

Overview

CH32V205 is an industrial-grade general-purpose microcontroller based on the QingKe RISC-V core. CH32V205 integrates a USB 2.0 high-speed PHY transceiver (480Mbps) and PD PHY, supporting PDUSB functionality. It includes USB Host and USB Device capabilities, USB PD, and Type-C fast charging. The device provides a programmable protocol I/O controller (PIOC), flash memory controller (FSMC), QSPI interface, CAN interface, 8 USARTs, 2 I2C interfaces, 2 SPI interfaces, multiple timer units, 2 OPAs, 2 CMPs, 4Msps high-speed 12-bit ADC, and 16 Touchkey channels.

Features

- **Core:**
  - QingKe RISC-V3B core, RV32ICBM-X instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - 2-level hardware interrupt stack
  - Conflict handling mechanism
  - System main frequency 192MHz
- **Memory:**
  - 32KB volatile data storage area SRAM
  - 256KB program memory CodeFlash
  - 3328KB BootLoader
  - 256B non-volatile system configuration memory
  - 256B user-defined memory
- **Power management and low-power consumption:**
  - System power supply V_{DD} voltage range: 1.8 to 3.6V
  - Independent power supply V_{IO} voltage range: 1.45 to 3.6V
  - Low-power mode: Sleep, Stop, Standby
  - V_{BAT} independently powers RTC and backup register
- **Clock & Reset**
  - Built-in factory-trimmed 8MHz RC oscillator
  - Built-in 40KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 192MHz
  - High-speed external 3~25MHz oscillator
  - Low-speed external 32.768 KHz oscillator
  - Power on/down reset, programmable voltage detector
- **2 sets of 16-channel general-purpose DMA controller**
  - 16 channels, support ring buffer
- **Programmable protocol I/O controller (PIOC)**
  - Programmable, supporting multiple 1-wire interfaces and 2-wire interfaces
- **2 sets of analog CMP：**
  - 2 input channels each, with optional internal reference voltage
  - Output to I/O or internal direct triggering of TIM
- **2 sets of OPA/PGA/CMP**
  - Multiple input channels, selectable multi-stage gain
  - Multiple output channels, selectable ADC pins
- **High-speed 12-bit ADC**
  - Analog input range: V_{SSA}~V_{DDA}
  - 16 external signals + 3 internal signals
  - On-chip temperature sensor
- **16-channels Touchkey detection**
- **Real-time clock (RTC):** 32-bit independent timer
- **Multiple timers**
  - 1×16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 2×16-bit general-purpose timers
  - 1×32-bit general-purpose timer
  - 2 watchdog timers (independent watchdog and window watchdog)

- SysTick: 32-bit counter

- **8 sets of USART: support LIN and ISO7816**
- **2 sets of I2C interface: Support SMBus/PMBus**
- **2 sets of SPI interface**
- **QuadSPI interface**
- **Flexible Static Memory Controller (FSMC)**
- **CAN interface (2.0B active)**
- **USB 2.0 full-speed controller and PHY：**

- Support USB host or USB device, single-wire USB

- **USB 2.0 high-speed Controller and PHY:**

- Support 480Mbps high-speed USB host or USB device

- Support USART serial port or I2C pin mapping

- USB PD and Type-C Controller and PHY:

- Support DRP, Sink, and Source applications; PDUSB

- Support PD3.2 and EPR; 100W or 240W fast charging

- **Fast GPIO port**

- 80 I/O ports, mapping 16 external interrupts

- **Security features: Chip unique ID**
- **Debug mode: 1-wire (default)/2-wire serial debug interface (SDI)**
- **Package: LQFP**

Resource difference \ Model		CH32V205			CH32V203
		CCT6	RCT6	VCT6	CCT6
Chip pin number		48	64	100	48
Flash (Bytes)		256K	256K	256K	256K
SRAM (Bytes)		32K	32K	32K	32K
GPIO port number		41	51	80	37
Timer	Advanced-control TIM1 (16-bit)	1	1	1	1
	General-purpose TIM2/3 (16-bit)	2	2	2	2
	General-purpose TIM4 (32-bit)	1	1	1	1
	Watchdog	2(WWDG+IWDG)			
	SysTick (32-bit)	√			√
RTC		√			√
ADC		16+3	16+3	16+3	10+3
TKEY		16-channel	16-channel	16-channel	10-channel
OPA		2	2	2	2
CMP		2	2	2	2
USART		8	8	8	8
SPI		2	2	2	2
I2C		2	2	2	2
CAN		1	1	1	1
QSPI		1	1	1	1
FSMC		-	-	1	-
PIOC		1	1	1	-
PDUSB	USBFS	1	1	1	1
	USBHS	1	1	1	-
	USB PD Type-C	1	1	1	-
CPU main frequency		40MHz@Zero-wait; Max: 192MHz@Non-zero wait			
Rated voltage		3.3V			
Operating temperature		Industrial-grade: -40℃~85℃			
Package form		LQFP48	LQFP64	LQFP100	LQFP48

Note: For the product with the fifth lot number of 0, the functions of CAN and USBPD are not provided.

Chapter 1 Specification Information

1.1 System Architecture

The microcontroller is based on the RISC-V instruction set architecture (ISA) in which the core, arbitration unit, DMA module, SRAM storage and other parts are interacted through multiple sets of buses. A general-purpose DMA controller is integrated in the chip to reduce the burden on the CPU and improve access efficiency. The application of a multi-level clock management mechanism reduces the operating power consumption of peripherals. At the same time, it has a data protection mechanism and measures such as automatic clock switching protection to increase system stability. The following figure is a block diagram of the overall internal structure of the series of products.

Figure 1-1-1 CH32V205 System block diagram

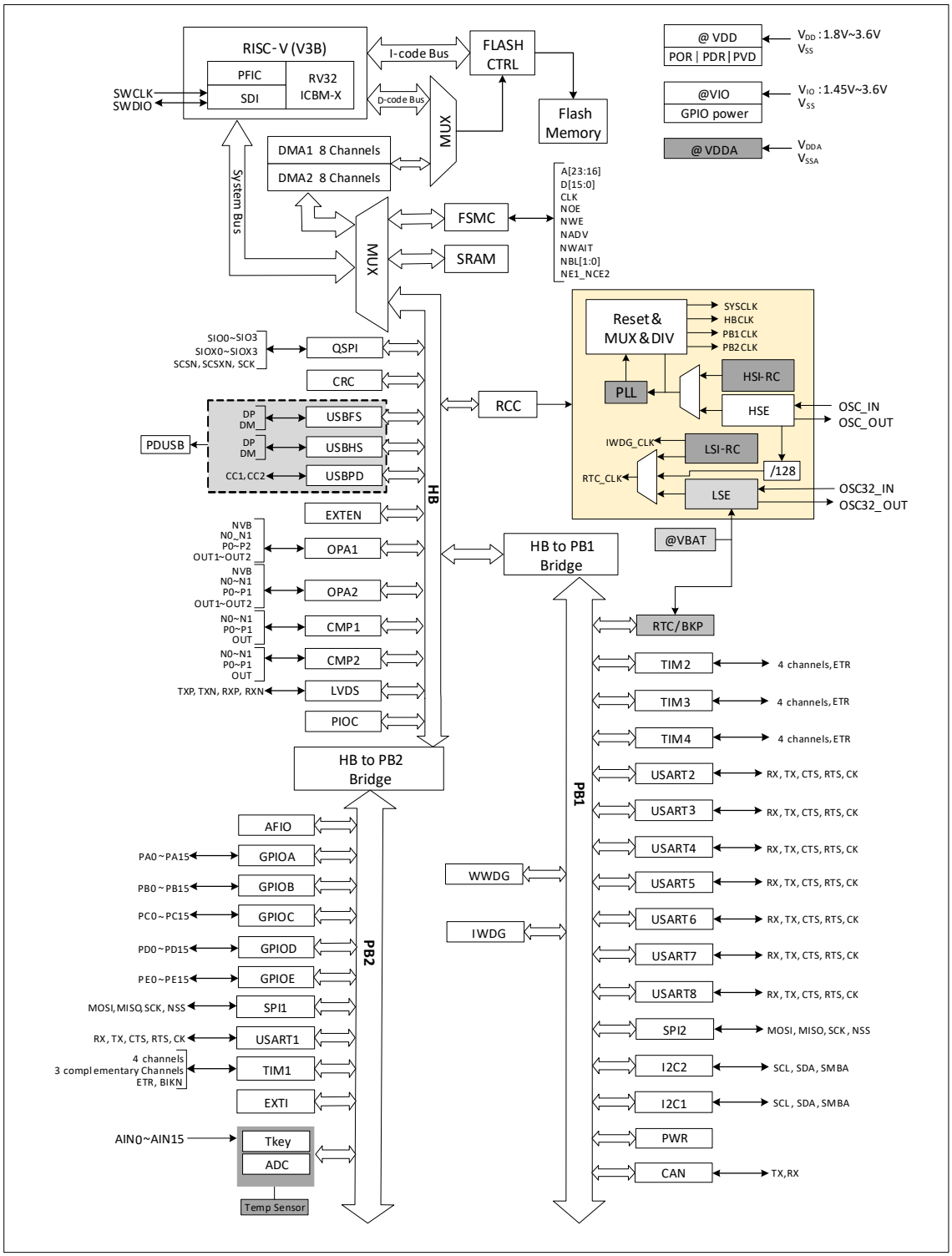
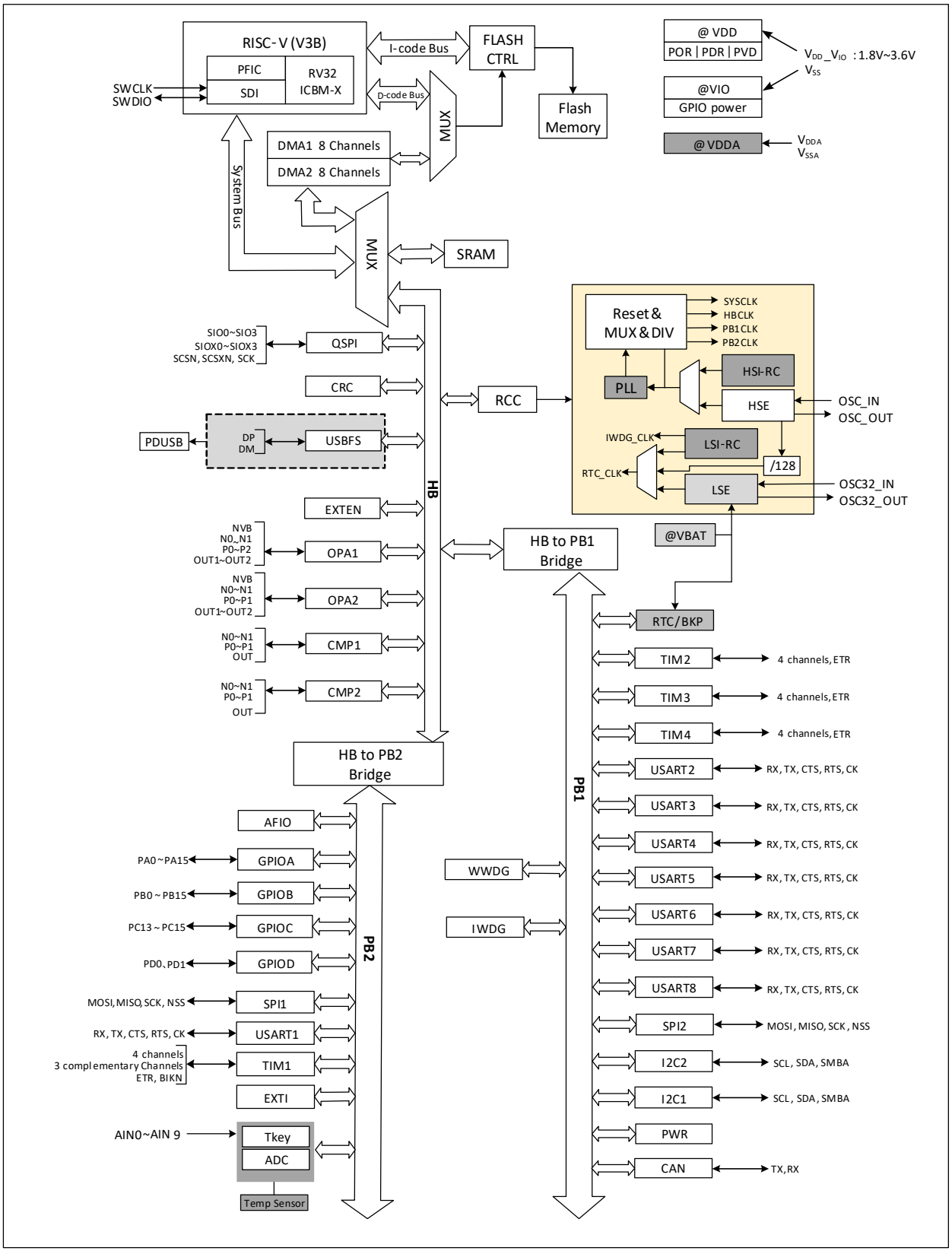
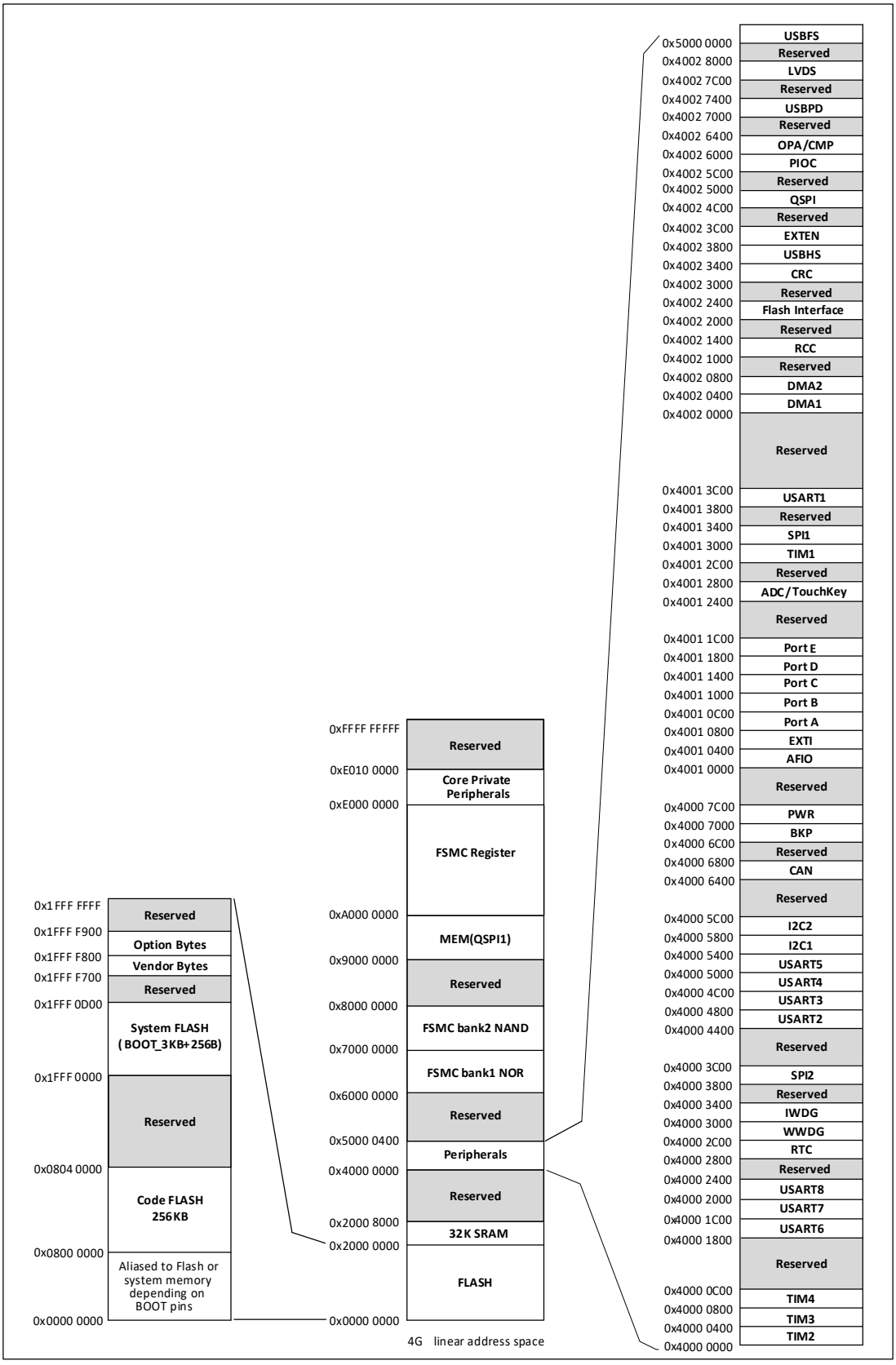


Figure 1-1-2 CH32V203 System block diagram



1.2 Memory Map

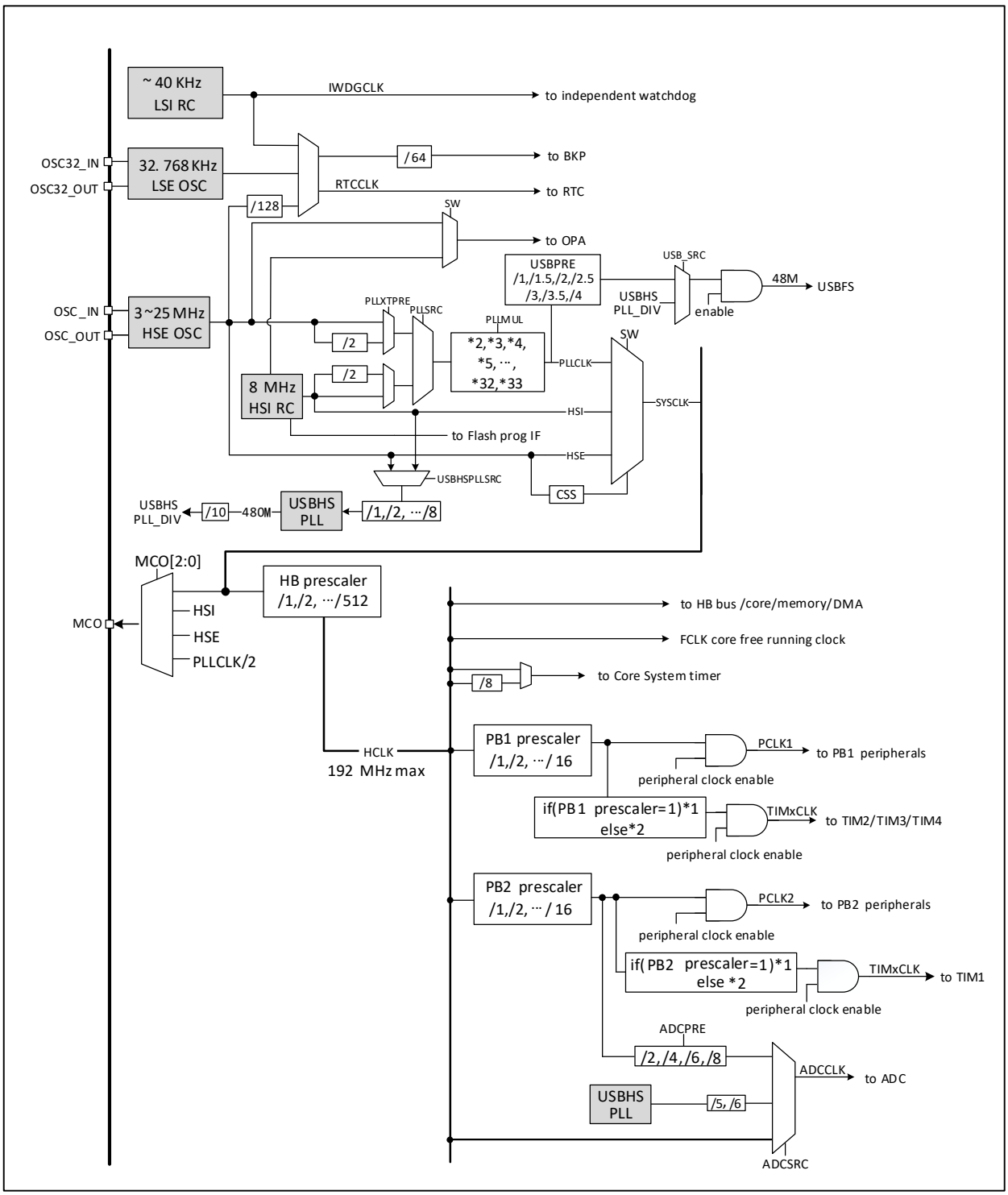
Figure 1-2 Memory address map



1.3 Clock Tree

4 groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and output as the system clock (SYSCLK). The system clock is then provided by each prescaler to provide the HB domain, PB1 domain, PB2 domain peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V3B Processor

RISC-V3B supports the ICBM-X subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as fast programmable interrupt controller (PFIC) and extended instruction support. Externally multiple buses are connected to external unit modules to enable interaction between external function modules and the core.

The processor can be flexibly applied in different scenarios, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc., due to its minimal instruction set, multiple working modes, and modular customization extensions.

- Support machine and user privilege mode
- Fast Programmable Interrupt Controller (PFIC)
- Multi-level hardware interrupt stack
- 1-wire/2-wire SDI
- Efficient jump, conflict detection
- Custom extended instructions

1.4.2 Programmable Protocol I/O Controller (PIOC)

The programmable protocol I/O controller is based on a special RISC core with a single clock cycle, which runs at the main frequency of the system. It has a program ROM with 2K instructions, 49 SFR registers and a PWM timer/counter, and supports the protocol control of 2 I/O pins.

- RISC core with optimized single-cycle bit-manipulation instruction set and fully static instruction set
- Reuse 4KB system SRAM as 2KB program ROM, supporting program suspension and dynamic loading
- Provide 33 registers (1 bidirectional and 1 unidirectional each), with 6 independent stacks
- Support 2 general-purpose bidirectional I/O protocol controllers with input level change detection
- Enables 1-wire and 2-wire interfaces for multiple protocol specifications via dynamic loading of protocol programs
- Support 1024-level serial connection for 1-wire ARGB chips

1.4.3 On-chip Memory and Boot Mode

Built-in 32Kbytes SRAM, available for storing data, which will be lost after power down. Among them, 4K(0x20000000-0x20000FFF) can be used for PIOC.

Built-in 64Kbytes program flash memory storage area (Code FLASH), i.e. user area, for user's application program and constant data storage. The specific size of the area corresponds to the chip model.

Built-in 3328 bytes System FLASH (System FLASH), i.e. BOOT area, used for system boot program storage, built-in bootstrap loading program.

Built-in 256 bytes system non-volatile configuration information storage area, used for vendor's configuration word storage, factory-cured, user cannot be modified.

Built-in 256 bytes user-defined information storage area for user option byte storage.

At startup, one of three bootstrap modes can be selected via the bootstrap pins (BOOT0 and BOOT1):

- Bootstrap from program flash memory
- Boot from system memory

- Boot from internal SRAM

The bootstrap loading program is stored in the system memory and the contents of the program flash memory storage area can be reprogrammed via the USART2 and USB interfaces.

1.4.4 Power Supply Scheme

(1) CH32V205

- V_{DD} = 1.8~3.6V: It is recommended to supply power to some I/O pins and the system voltage regulator LDO, including the built-in USB2.0. It is recommended to connect 0.1uF high-frequency capacitors externally, and it is recommended to connect a 4.7uF capacitor in parallel to the whole V_{DD} power supply. When used in communication interfaces such as USB2.0, the recommended V_{DD} range is 3.15~3.45V.
- V_{IO} = 1.45~3.6V: Supplies power to some standard I/O pins, determining the high-voltage output amplitude of the pins. It is recommended to connect a 0.1uF high-frequency capacitor to each pin. Additionally, a 4.7uF capacitor should be connected in parallel across the entire V_{IO} power supply. During normal operation, the V_{IO} voltage must not exceed the V_{DD} voltage, nor must it exceed the V_{DDA} voltage.
- V_{DDA} = 1.8~3.6V: Supplies power to the analog portion of the high-frequency RC oscillator, ADC, TKEY, OPA, CMP, TS, and PLL. During normal operation, the V_{DDA} voltage equals the V_{DD} voltage. When using an OPA, it is recommended that V_{DDA} and V_{IO} be set to the same voltage. When not using an OPA, V_{DDA} may be higher than the V_{IO} voltage. When using an ADC, it is recommended that V_{DDA} not be lower than 2.4V. When using TKEY, the V_{IO} voltage must not exceed the V_{DDA} voltage, and it is recommended that V_{DDA} not be lower than 2.4V.
- V_{BAT} = 1.8~3.6V: Optional backup power supply. When V_{DD} is turned off, the internal power switch switches to V_{BAT} to provide power exclusively to the RTC and external low-frequency oscillator.
- V_{REF+} = 1.8~3.6V: Reference voltage for the ADC. An external high-frequency capacitor with a capacitance of 0.1uF is recommended. V_{REF+} must not exceed the V_{DDA} voltage.

The power pins with the same names above must be shorted. The voltage relationship is: $V_{DD} = V_{DDA} \geq V_{IO}$; and $V_{DDA} \geq V_{REF+}$.

(2) CH32V203

- V_{DD_IO} = 1.8~3.6V: It is recommended to supply power to some I/O pins and the system voltage regulator LDO, including the built-in USBFS. It is recommended to connect 0.1uF high-frequency capacitors externally, and it is recommended to connect a 4.7uF capacitor in parallel to the whole V_{DD_IO} power supply. When used in communication interfaces such as USBFS, the recommended V_{DD} range is 3.15~3.45V.
- V_{DDA} = 1.8~3.6V: Supplies power to the analog portion of the high-frequency RC oscillator, ADC, TKEY, OPA, CMP, TS, and PLL. When using an ADC, it is recommended that V_{DDA} not be lower than 2.4V.
- V_{BAT} = 1.8~3.6V: Optional backup power supply. When V_{DD} is turned off, the internal power switch switches to V_{BAT} to provide power exclusively to the RTC and external low-frequency oscillator.

The power pins with the same names above must be shorted. The voltage relationship is: $V_{DD\_IO} = V_{DDA}$.

1.4.5 Power Supply Detector

The chip integrates a power-on reset (POR)/power-off reset (PDR) circuit, which is always in a working state to ensure that the system works when the power supply is not less than 1.8V; when V_{DD} falls below the set

threshold ($V_{POR/PDR}$), it puts the device in reset without the need for an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage magnitude of the V_{DD} supply with the set threshold V_{PVD}. Turning on the corresponding edge interrupt of the PVD allows you to receive an interrupt notification when V_{DD} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for $V_{POR/PDR}$ and V_{PVD} values.

1.4.6 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are 3 modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.
- Shutdown mode: The regulator is automatically switched to this mode when the CPU enters the Standby mode, the regulator output is high resistance, the power supply to the core circuit is cut off, and the regulator is in the zero-consumption state.

The regulator is always in on mode after reset, and is turned off in standby mode in shutdown mode, when it is high resistance output.

1.4.7 Low-power Mode

The system supports 3 low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

This mode FLASH enters the low-power mode or power-off state, and the RC oscillator and HSE crystal oscillator of PLL and HSI are turned off. The stop mode can achieve the lowest power consumption while keeping the contents of SRAM and registers intact.

The stop mode is divided into 4 cases: Stop Mode 1, Stop Mode 2, Stop Mode 3 and Stop Mode 4. For detailed information, please refer to the Low-power Mode related chapter in the CH32V205RM manual.

Exit condition: Any external interrupt / event (EXTI signal), WKUP pin rising edge, external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 80 external I/O ports, PVD output, RTC alarm clock, USB wake-up signal, USB PD wake-up signal, CMP wake-up signal and so on.

- Standby mode (STANDBY)

In this mode, the main LDO of the system is turned off, the wake-up circuit is powered by the low-power LDO, all other digital circuits are powered off, and the FLASH is in a power-off state. The wake-up system from standby mode will reset and SBF (PWR_CSR) will be set. After waking up, the SBF status is queried to know the low-power mode before wake-up, and the SBF is cleared by the CSBF (PWR_CR) bit. In standby mode, the contents of 32KB's SRAM can be maintained (depending on the planned configuration before going to bed), and the contents of the backup register can be retained.

Exit conditions: EXT10~EXT17 any external event (excluding interrupts), rising edge on WKUP, external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 80 external I/O ports, RTC alarm clock, etc.

1.4.8 CRC (cyclic redundancy check) Calculation Unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, a means of detecting flash errors is provided. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

1.4.9 Programmable Fast Interrupt controller (PFIC)

The product has a built-in Programmable Fast Interrupt Controller (PFIC), which supports up to 256 interrupt vectors, and provides flexible interrupt management functions with minimal interrupt latency. The current product manages 7 core private interrupts and 67 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in user and machine privileged modes.

- A non-maskable interrupt NMI
- Support hardware interrupt stack (HPE) without instruction overhead
- 4-channel vector table free interrupts (VTF)
- Vector table supports address or command mode
- Configurable interrupt nesting depth, up to 2 levels
- Support interrupt tail-chaining

1.4.10 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 23 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal PB2. Up to 80 general-purpose I/O ports can be connected to 16 external interrupt lines.

1.4.11 General DMA Controller

The system has built-in 2 groups of general-purpose DMA controllers, manages 16 channels in total, including 8 channels in DMA1 and 8 channels in DMA2. Flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general/advanced TIMx, ADC, USART, I2C, SPI, QSPI.

Note: DMA1, DMA2 and CPU access the system SRAM after arbitration by the arbiter.

1.4.12 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 3~25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock

(directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of HB. The high-speed PB (PB2) and low-speed PB (PB1) regions provide peripheral clocks with a maximum frequency of 144MHz. Refer to the clock tree block diagram in Figure 1-3.

1.4.13 Real Time Clock (RTC) and Backup Registers

The RTC and the backup register are in the backup power supply area inside the system. When V_{DD} is valid, it is powered by V_{DD}, and when V_{DD} is invalid, the internal power is automatically switched to the V_{BAT} pin.

RTC is a set of 32-bit programmable counters, and its time base supports 20-bit prescaler, which is used for long-time measurement. The clock reference comes from high-speed external clock (HSE/128) 128 frequency division, external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the setting and time of RTC can remain unchanged after the system is reset or awakened from standby mode.

The backup register contains up to 10×16-bit registers, which can be used to store 20 bytes of user application data. This data can continue to be maintained after wake-up from Standby, or system Reset or power Reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

1.4.14 Analog-to-digital Converter (ADC) and Touchkey Capacitance Detection (TouchKey)

The chip has a built-in 12-bit ADC that provides up to 16 external channels and 3 internal channel samples with programmable channel sampling times for single, continuous, sweep or intermittent conversion. Provides analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages, provides configurable analog watchdog reset function to reset the system when monitored voltage exceeds a threshold. Supports external event-triggered transitions. Trigger sources include internal signals from on-chip timers and external pins. Supports operation using DMA.

The internal channels of the ADC are ADC_IN16~ADC_IN18. The temperature sensor is internally connected to the IN16 input channel for converting the sensor output to a digital value; the internal reference voltage is connected to the IN17 input channel; and $V_{DDA}/2$ is connected to the IN18 input channel.

The touch-key capacitance detection unit provides up to 16 detection channels and reuses the external channels of the ADC module. The detection result is converted into the output result by the ADC module, and the touch-key state is identified by the user software.

1.4.15 Timer and Watchdog

- Advanced-control timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a 3-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have

the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer (TIM2/3/4)

The general-purpose timer is two 16-bit (TIM2, TIM3) and 1 32-bit (TIM4) autoload add / decrement counters with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation, and single pulse mode output. It can also work with advanced control timers through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen while PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Any general timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process the signal of the incremental encoder and the digital output of 1 to 3 Hall sensors.

- Independent watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 40KHz. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window watchdog (WWDG)

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- System time base timer (SysTick)

QingKe microprocessor core comes with a 32-bit optional increment or decrement counter, which is used to generate SYSTICK exceptions (exception number: 12), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, or can be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.16 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 8 sets of Universal Synchronous/Asynchronous Transceivers (USART1/2/3/4/5/6/7/8). Full duplex asynchronous communication, synchronous unidirectional communication, and half duplex single line communication are supported, as well as LIN (Local Interconnect Network), ISO7816 compatible smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation for continuous communication.

1.4.17 Serial Peripheral Interface (SPI)

Up to 2 groups of serial peripherals interface (SPI1/2) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

1.4.18 QSPI Interface

A set of dedicated QSPI communication interfaces (QuadSPI) is built into the chip, which is connected with single, double or four (data lines) SPI FLASH storage media. The main features are:

- 3 functional modes: Indirect mode, Status polling mode, and Memory-mapped mode
- Dual flash mode via parallel access to two FLASH devices
- Integrated FIFOs for transmission and reception
- Support SDR mode
- Fully programmable frame format for indirect and memory-mapped modes
- Fully programmable opcode for indirect and memory-mapped modes
- Generate DMA trigger signals upon reaching FIFO threshold and transmission completion
- Generate interrupts upon reaching FIFO threshold, timeout, operation completion, and access errors

1.4.19 I2C Bus

Up to 2 I2C bus interfaces can work in multi-master mode or Slave mode, perform all I²C Bus specific timing, protocol, arbitration, etc. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0/PMBus bus.

1.4.20 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and it supports time-triggered communication functions. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and two 3-level deep receiving FIFOs.

1.4.21 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS)

The USB2.0 full-speed host controller and device controller (USBFS) follow the USB2.0 full-speed standard. It provides 8 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up functions.

1.4.22 Universal Serial Bus USB2.0 High-speed Host/Device Controller (USBHS)

The USB2.0 high-speed controller has the dual roles of host controller and device controller, and has a built-in USB-PHY physical layer transceiver of 480Mbps. When used as a host controller, it can support low-speed, full-speed and high-speed USB devices. When used as a device controller, it can be flexibly set to low speed, full speed or high-speed mode to adapt to various applications. The main features include:

- Support USB 2.1, USB 2.0, USB 1.1, and USB 1.0 protocol specifications
- Support USB Host and USB Device functionality
- Support control transfers, bulk transfers, interrupt transfers, and real-time/synchronous transfers
- Provide bus reset, suspend, wake-up, and resume functions
- Host supports high-speed USB hub
- All non-zero endpoints support up to 1024-byte packets with built-in FIFO, supporting interrupts and DMA
- Support USART serial port or I2C pin mapping

1.4.23 USB PD and Type-C Controller (USB PD)

Built-in USB Power Delivery controller and PD physical layer transceiver PHY support USB Type-C master-slave detection, automatic BMC codec and CRC, and CC pin supports hardware edge control.

Support USB PD2.0 and PD3.0 and PD3.2 power transmission, support SPR and EPR, support 100W or 240W fast charging, support PD power receiving terminal Sink and PD power supply terminal Source and DRP application. Support PDUSB, UFP, DFP and DRD applications.

1.4.24 Flexible Static Memory Controller (FSMC)

The FSMC interface mainly provides synchronous or asynchronous memory interfaces and supports SRAM, PSRAM, NOR and NAND devices. The internal HB transmission signal is converted into an appropriate external communication protocol, allowing continuous access of 8/16/32 bits of data. And that sample delay time can be flexibly configured to meet the time sequence of different devices.

In addition, FSMC can also be used for most graphic LCD controller interfaces, supporting the modes of Intel 8080 and Motorola 6800, facilitating the construction of a simple graphic application environment, or for a high-performance scheme of a special acceleration controller.

1.4.25 General-purpose Input and Output (GPIO)

The system provides 5 groups of GPIO ports (PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15) with a total of 80 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the IO configuration to avoid accidental writing to the I/O register.

Most of the I/O pins in the system are provided by $V_{I/O}$. Changing the $V_{I/O}$ power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. PA11, PA12, PB6, PB7, PE2 to PE5 are powered by V_{DD}. PC13 to PC15 are powered by either V_{DD} or V_{BAT}. Please refer to the pin description for specific pins.

1.4.26 Operational Amplifier (OPA)

The chip integrates 2 operational amplifiers (OPA1/2) that can function as voltage comparators, supporting programmable gain amplifier (PGA) for selectable amplification. Its inputs can be configured to select multiple channels, enabling automatic multi-channel polling. Its outputs can be configured to select two channels, internally linked to ADC and CMP input channels, supporting amplification of external analog small signals before conversion by the ADC.

1.4.27 Voltage Comparators (CMP)

The chip incorporates 2 sets of rail-to-rail universal voltage comparators, supporting selectable hysteresis characteristics and digital filtering. Voltage comparison results are output via GPIO or directly connected internally to trigger input channels: TIM1's CH4, TIM2's CH3–CH4, TIM3's CH4, and TIM4's CH3~CH4.

1.4.28 Serial Debug Interface (SDI)

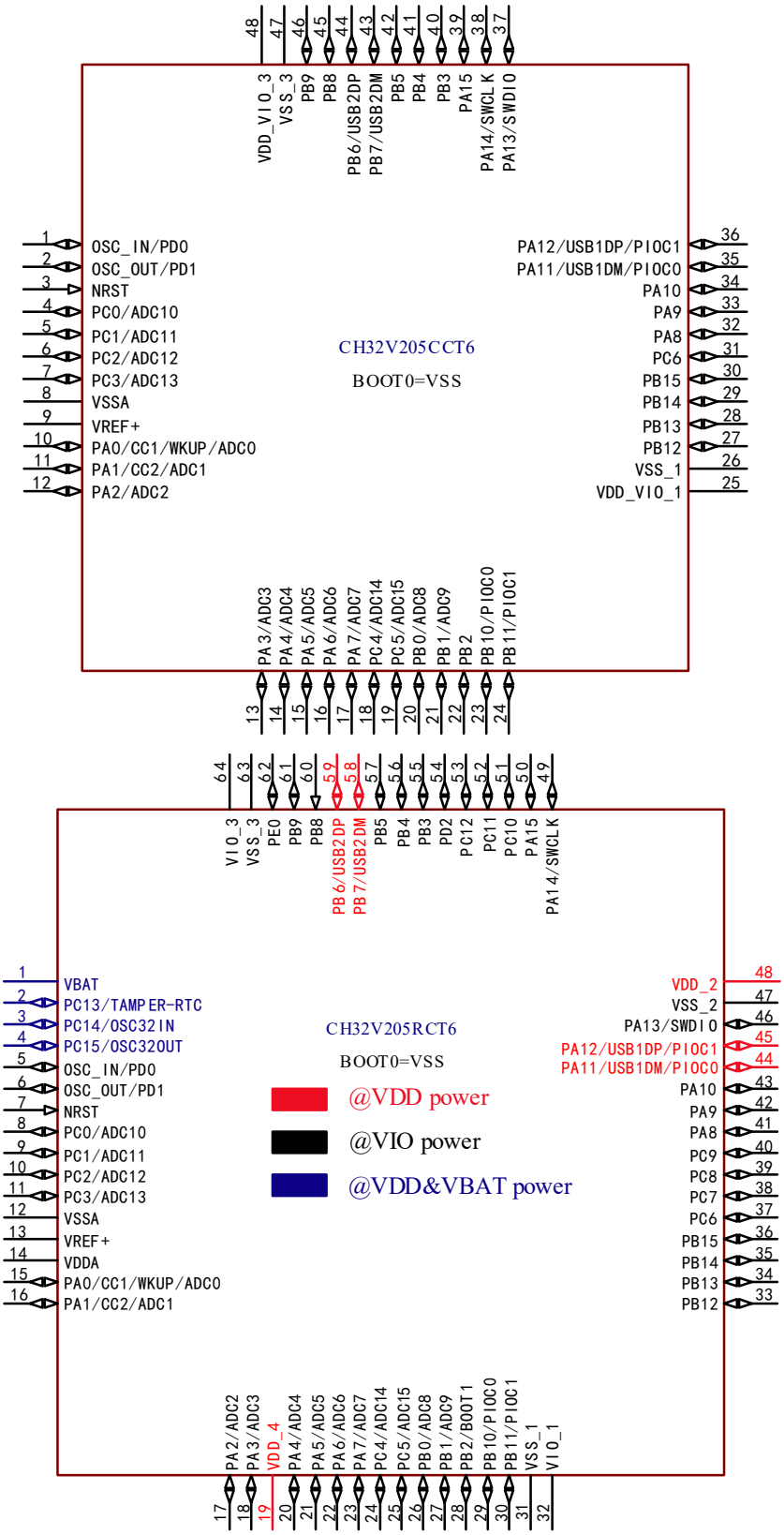
The core includes a built-in 1-wire SDI Serial Debug Interface and a 2-wire SDI Serial Debug Interface. The system supports both 1-wire and 2-wire debug modes. 1-wire debugging is the default mode, utilizing the

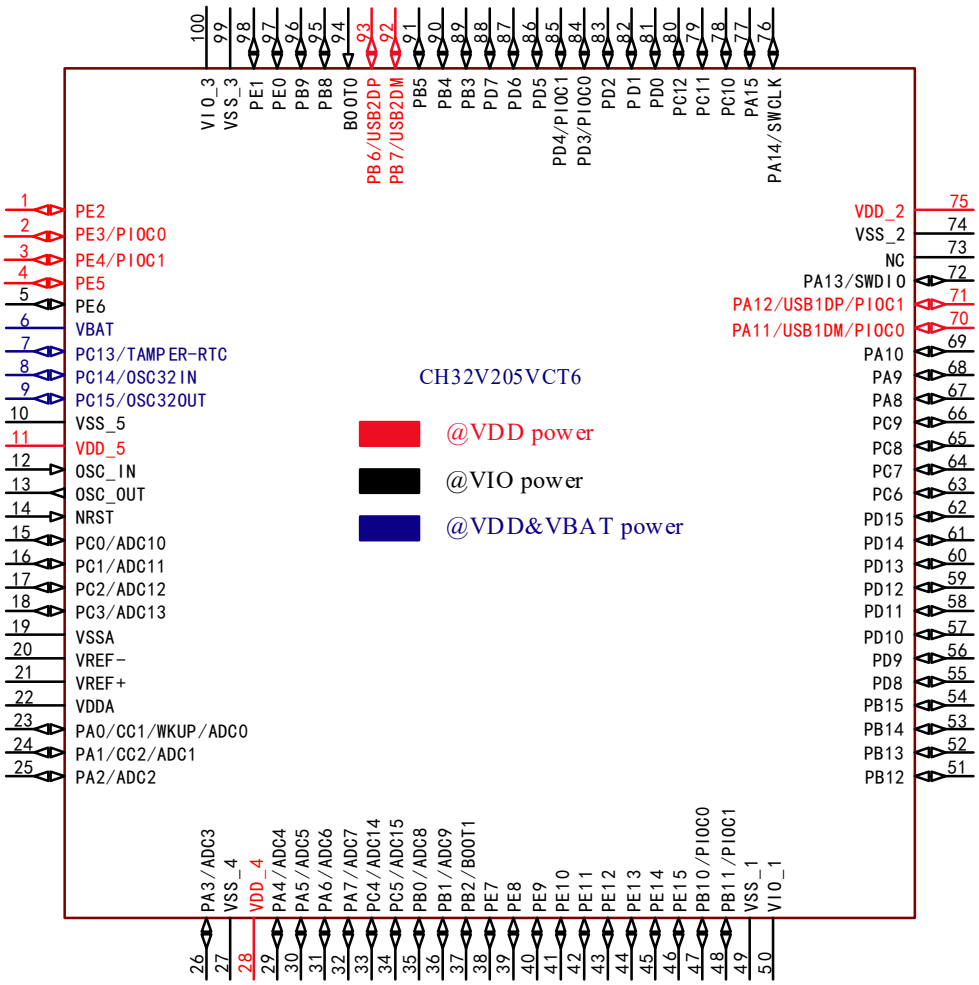
SWIO pin (Single Wire Input Output). 2-wire debugging employs the SWDIO and SWCLK pins, enhancing download speeds during application. Upon power-up or reset, the debug interface pins default to active functionality. After the main program runs, SDI can be disabled as needed.

Chapter 2 Pinouts and Pin Definition

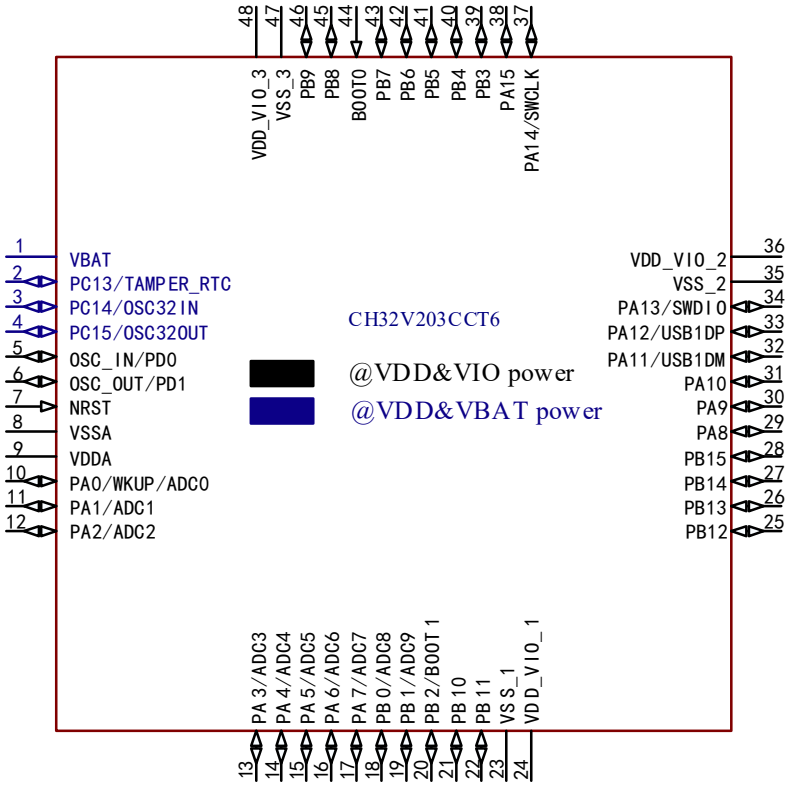
2.1 Pinout

2.1.1 CH32V205 Pinouts




CH32V205VCT6
@VDD power
@VIO power
@VDD&VBAT power
1 PE2
2 PE3/PIOC0
3 PE4/PIOC1
4 PE5
5 PE6
6 VBAT
7 PC13/TAMPER-RTC
8 PC14/OSC32IN
9 PC15/OSC32OUT
10 VSS_5
11 VDD_5
12 OSC_IN
13 OSC_OUT
14 NRST
15 PC0/ADC10
16 PC1/ADC11
17 PC2/ADC12
18 PC3/ADC13
19 VSSA
20 VREF-
21 VREF+
22 VDDA
23 PA0/CC1/WKUP/ADC0
24 PA1/CC2/ADC1
25 PA2/ADC2
26 PA3/ADC3
27 VSS_4
28 VDD_4
29 PA4/ADC4
30 PA5/ADC5
31 PA6/ADC6
32 PA7/ADC7
33 PC4/ADC14
34 PC5/ADC15
35 PB0/ADC8
36 PB1/ADC9
37 PB2/BOOT1
38 PE7
39 PE8
40 PE9
41 PE10
42 PE11
43 PE12
44 PE13
45 PE14
46 PE15
47 PB10/PIOC0
48 PB11/PIOC1
49 VSS_1
50 VIO_1
51 PB12
52 PB13
53 PB14
54 PB15
55 PD8
56 PD9
57 PD10
58 PD11
59 PD12
60 PD13
61 PD14
62 PD15
63 PC6
64 PC7
65 PC8
66 PC9
67 PA8
68 PA9
69 PA10
70 PA11/USB1DM/PIOC0
71 PA12/USB1DP/PIOC1
72 PA13/SWDIO
73 NC
74 VSS_2
75 VDD_2
76 PA14/SWCLK
77 PA15
78 PC10
79 PC11
80 PD0
81 PD1
82 PD2
83 PD3/PIOC0
84 PD4/PIOC1
85 PD5
86 PD6
87 PD7
88 PB3
89 PB4
90 PB5
91 PB7/USB2DM
92 PB6/USB2DP
93 BOOT0
94 PB8
95 PB9
96 PE0
97 PE1
98 VSS_3
99 VIO_3
100

2.1.2 CH32V203 Pinouts



Note: Multiplexed functions are abbreviated in the pin diagram.

Example:

ADC: (ADC0: ADC_IN0)

USB2DP: USBHS_DP

USB2DN: USBHS_DN

2.2 Pin Definitions

Note: The pin function in the table below refer to all functions and do not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 2-1-1 CH32V205 pin definitions

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
-	-	1	PE2	I/O	-	PE2	FSMC_ADDR23(AF7)	
-	-	2	PE3	I/O	-	PE3	PIOC_IO0(AF4)/ FSMC_ADDR19(AF7)	
-	-	3	PE4	I/O	-	PE4	PIOC_IO1(AF4)/ FSMC_ADDR20(AF7)	
-	-	4	PE5	I/O	-	PE5	FSMC_ADDR21(AF7)	
-	-	5	PE6	I/O	-	PE6	QSPI_SIO2(AF5)/ FSMC_ADDR22(AF7)	
-	1	6	V_{BAT}	P	-	V_{BAT}		
-	2	7	PC13-TAMPER-RTC (3)	I/O	-	PC13(4)	TAMPER/RTC/TIM1_CH4(AF0)/ I2C2_SCL(AF7)	
-	3	8	PC14-OSC32_IN(3)	I/O/A	-	PC14(4)	OSC32_IN/I2C2_SDA(AF7)	
-	4	9	PC15-OSC32_OUT(3)	I/O/A	-	PC15(4)	OSC32_OUT/I2C2_SMBA(AF7)	
-	-	10	V_{SS_5}	P	-	V_{SS_5}		
-	-	11	V_{DD_5}	P	-	V_{DD_5}		
3	7	14	NRST	I	-	NRST		
4	8	15	PC0	I/O/A	-	PC0	ADC_IN10/USART6_TX(AF2)	
5	9	16	PC1	I/O/A	-	PC1	ADC_IN11/USART6_RX(AF2)	
6	10	17	PC2	I/O/A	-	PC2	ADC_IN12/USART7_TX(AF2)/ USART6_CTS(AF4)	
7	11	18	PC3	I/O/A	-	PC3	ADC_IN13/TIM1_CH1N(AF0)/ USART7_RX(AF2)/ USART6_RTS(AF4)	
8	12	19	V_{SSA}	P	-	V_{SSA}		

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
-	-	20	V_{REF-}	P	-	V_{REF-}		
9	13	21	V_{REF+}	P	-	V_{REF+}		
-	14	22	V_{DDA}	P	-	V_{DDA}		
10	15	23	PA0-WKUP	I/O/A	FT	PA0	WKUP/ADC_IN0/ TIM1_ETR(AF0)/ TIM2_CH1_ETR(AF1)/ USART2_CTS(AF2)/ QSPI_SIO2(AF5)/CC1(AF7)	
11	16	24	PA1	I/O/A	FT	PA1	ADC_IN1/TIM2_CH2(AF1)/ USART2_RTS(AF2)/ QSPI_SIO3(AF5)/CC2(AF7)	
12	17	25	PA2	I/O/A	-	PA2	ADC_IN2/OPA2_OUT2/ CMP1_CHP0/TIM2_CH3(AF 1)/ USART2_TX(AF2)/ QSPI_SIO0(AF5)	
13	18	26	PA3	I/O/A	-	PA3	ADC_IN3/OPA1_OUT2/ TIM2_CH4(AF1)/ USART2_RX(AF2)/ QSPI_SIO1(AF5)	
-	-	27	V_{SS_4}	P	-	V_{SS_4}		
-	19	28	V_{DD_4}	P	-	V_{DD_4}		
14	20	29	PA4	I/O/A	-	PA4	ADC_IN4/OPA2_OUT1/ USART2_CK(AF2)/ SPI1_NSS(AF5)	
15	21	30	PA5	I/O/A	-	PA5	ADC_IN5/OPA2_CHN1/ USART1_CTS(AF2)/ USART1_CK(AF3)/ USART7_CK(AF4)/ SPI1_SCK(AF5)	
16	22	31	PA6	I/O/A	-	PA6	ADC_IN6/OPA1_CHN1/ TIM1_BK(AF0)/ TIM3_CH1(AF1)/ USART1_TX(AF2)/ USART7_TX(AF3)/ USART7_CTS(AF4)/ SPI1_MISO(AF5)	
17	23	32	PA7	I/O/A	-	PA7	ADC_IN7/OPA2_CHP1/ TIM1_CH1N(AF0)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							TIM3_CH2(AF1)/ USART1_RX(AF2)/ USART7_RX(AF3)/ USART7_RTS(AF4)/ SPI1_MOSI(AF5)	
18	24	33	PC4	I/O/A	-	PC4	ADC_IN14/TIM1_CH2N(AF0)/ USART1_CTS(AF2)/ USART8_TX(AF3)	
19	25	34	PC5	I/O/A	-	PC5	ADC_IN15/TIM1_CH3N(AF0)/ USART1_RTS(AF2)/ USART8_RX(AF3)	
20	26	35	PB0	I/O/A	-	PB0	ADC_IN8/OPA1_CHP1/ TIM1_CH2N(AF0)/ TIM3_CH3(AF1)/ USART4_TX(AF2)/ QSPI_SCSN(AF5) USART8_CTS(AF3)/	
21	27	36	PB1	I/O/A	-	PB1	ADC_IN9/USART8_RTS(AF3)/ OPA1_OUT1/TIM1_CH3N(AF0)/ TIM3_CH4(AF1)/ USART4_RX(AF2)/ CMP1_CHN0/QSPI_SCSXN(AF5)	
-	28	37	BOOT1	I	-	BOOT1		
22			PB2	I/O/A	-	PB2	CMP1_CHP1/USART5_TX(AF3)/ QSPI_SCK(AF5)	
-	-	38	PE7	I/O	-	PE7	TIM1_ETR(AF0)/ QSPI_SIOX0(AF5)/ FSMC_D4(AF7)	
-	-	39	PE8	I/O	-	PE8	TIM1_CH1N(AF0)/ USART5_TX(AF2)/ QSPI_SIOX1(AF5)/ FSMC_D5(AF7)	
-	-	40	PE9	I/O	-	PE9	TIM1_CH1(AF0)/ USART5_RX(AF2)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							QSPI_SIOX2(AF5)/ FSMC_D6(AF7)	
-	-	41	PE10	I/O	-	PE10	TIM1_CH2N(AF0)/ USART6_TX(AF2)/ QSPI_SIOX3(AF5)/ FSMC_D7(AF7)	
-	-	42	PE11	I/O	FT	PE11	TIM1_CH2(AF0)/ USART6_RX(AF2)/ FSMC_D8(AF7)	
-	-	43	PE12	I/O	FT	PE12	TIM1_CH3N(AF0)/ USART7_TX(AF2)/ FSMC_D9(AF7)	
-	-	44	PE13	I/O	FT	PE13	TIM1_CH3(AF0)/ USART7_RX(AF2)/ FSMC_D10(AF7)	
-	-	45	PE14	I/O	FT	PE14	TIM1_CH4(AF0)/ USART8_TX(AF2)/ FSMC_D11(AF7)	
-	-	46	PE15	I/O	FT	PE15	TIM1_BK(AF0)/ USART8_RX(AF2)/ FSMC_D12(AF7)	
23	29	47	PB10	I/O/A	-	PB10	OPA2_CHN0/TIM2_CH3(AF 1)/ USART3_TX(AF2)/ PIOC_IO0(AF4)/ QSPI_SIOX2(AF5)/ I2C2_SCL(AF7)	
24	30	48	PB11	I/O/A	-	PB11	OPA1_CHN0/CMP2_CHN1/ TIM2_CH4(AF1)/ USART3_RX(AF2)/ PIOC_IO1(AF4)/ I2C2_SDA(AF7)/ QSPI_SIOX3(AF5)	
26	31	49	V_{SS_1}	P	-	V_{SS_1}		
-	32	50	V_{IO_1}	P	-	V_{IO_1}		
25	-	-	$V_{DD\_V_{IO\_1}}$	P	-	$V_{DD\_V_{IO\_1}}$		
27	33	51	PB12	I/O/A	-	PB12	OPA1_CHP2/TIM1_BK(AF0) / CMP1_OUT(AF1)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							USART3_CK(AF2)/ USART4_CTS(AF3)/ SPI2_NSS(AF5)/ I2C2_SMBA(AF7)	
28	34	52	PB13	I/O/A	-	PB13	OPA1_CHNVB/ TIM1_CH1N(AF0)/ USART3_CTS(AF2)/ SPI2_SCK(AF5)	
29	35	53	PB14	I/O/A	-	PB14	OPA2_CHP0/TIM1_CH2N(AF0)/ USART3_RTS(AF2)/ SPI2_MISO(AF5)	
30	36	54	PB15	I/O/A	-	PB15	OPA2_CHNVB/ TIM1_CH3N(AF0)/ USART1_TX(AF2)/ USART4_RTS(AF3)/ USART6_CK(AF4)/ SPI2_MOSI(AF5)	
-	-	55	PD8	I/O	FT	PD8	USART3_TX(AF2)/ FSMC_D13(AF7)	
-	-	56	PD9	I/O	FT	PD9	USART3_RX(AF2)/ FSMC_D14(AF7)	
-	-	57	PD10	I/O	FT	PD10	USART3_CK(AF2)/ FSMC_D15(AF7)	
-	-	58	PD11	I/O	-	PD11	USART3_CTS(AF2)/ QSPI_SIO0(AF5)/ FSMC_ADDR16(AF7)	
-	-	59	PD12	I/O	-	PD12	TIM4_CH1(AF1)/ USART3_RTS(AF2)/ QSPI_SIO1(AF5)/ FSMC_ADDR17(AF7)	
-	-	60	PD13	I/O	-	PD13	TIM4_CH2(AF1)/ QSPI_SIO3(AF5)/ FSMC_ADDR18(AF7)	
-	-	61	PD14	I/O	FT	PD14	TIM4_CH3(AF1)/ FSMC_D0(AF7)	
-	-	62	PD15	I/O	FT	PD15	TIM4_CH4(AF1)/ FSMC_D1(AF7)	
31	37	63	PC6	I/O	FT	PC6	TIM1_CH1(AF0)/ TIM3_CH1(AF1)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							USART7_TX(AF4)	
-	38	64	PC7	I/O	FT	PC7	TIM1_CH2(AF0)/ TIM3_CH2(AF1)/ USART7_RX(AF4)	
-	39	65	PC8	I/O	FT	PC8	TIM1_CH3(AF0)/ TIM3_CH3(AF1)/ USART5_CK(AF4)	
-	40	66	PC9	I/O	-	PC9	TIM1_CH4(AF0)/ TIM3_CH4(AF1)/ USART8_TX(AF4)/ QSPI_SIO0(AF5)	
32	41	67	PA8	I/O/A	-	PA8	CMP2_CHP1/TIM1_CH1(AF0)/ USART1_CK(AF2)/ USART1_RX(AF3)/MCO(AF6)	
33	42	68	PA9	I/O/A	-	PA9	CMP2_CHN0/TIM1_CH2(AF0)/ USART1_TX(AF2)/ USART1_RTS(AF3)	
34	43	69	PA10	I/O	FT	PA10	TIM1_CH3(AF0)/ USART1_RX(AF2)/ USART1_CK(AF3)	
35	44	70	PA11	I/O	FT	PA11	USBFS_DM/TIM1_CH4(AF0)/ USART1_CTS(AF2)/ USART1_TX(AF3)/ PIOC_IO0(AF4)/CAN_RX(AF6)	
36	45	71	PA12	I/O	FT	PA12	USBFS_DP/TIM1_ETR(AF0)/ CMP2_OUT(AF1)/ USART1_RTS(AF2)/ USART6_TX(AF3)/ PIOC_IO1(AF4)/ QSPI_SCK(AF5)/CAN_TX(AF6)	
37	46	72	PA13	I/O	FT	PA13	SWDIO/TIM1_CH1N(AF0)/ TIM2_CH3(AF1)/ USART3_TX(AF2)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							I2C1_SDA(AF7)	
-	-	73	NC.	-	-	-		
-	47	74	V_{SS_2}	P	-	V_{SS_2}		
-	48	75	V_{DD_2}	P	-	V_{DD_2}		
38	49	76	PA14	I/O	FT	PA14	SWCLK/TIM1_CH2N(AF0)/ TIM2_CH4(AF1)/ USART8_TX(AF2)/ USART3_RX(AF3)/ USART4_TX(AF4)/ I2C1_SCL(AF7)	
39	50	77	PA15	I/O	-	PA15	TIM1_CH3N(AF0)/ TIM2_CH1_ETR(AF1)/ USART8_RX(AF2)/ USART8_CK(AF3)/ USART4_RX(AF4)/ SPI1_NSS(AF5)	
-	51	78	PC10	I/O	-	PC10	TIM1_CH1(AF0)/ USART3_TX(AF2)/ USART4_TX(AF3)/ QSPI_SIO1(AF5)	
-	52	79	PC11	I/O	-	PC11	TIM1_CH2(AF0)/ USART3_RX(AF2)/ USART4_RX(AF3)/ QSPI_SCSXN(AF5)	
-	53	80	PC12	I/O	FT	PC12	TIM1_CH3(AF0)/ USART3_CK(AF2)/ USART5_TX(AF3)/ USART8_RX(AF4)	
1	5	12	OSC_IN	I/A	-	OSC_IN		PD0(6)
		81	PD0(6)(7)	I/O	FT	PD0	USART4_CK(AF3)/ CAN_RX(AF6)/ FSMC_D2(AF7)	
2	6	13	OSC_OUT	O/A	-	OSC_OUT		PD1(6)
		82	PD1(6)	I/O	FT	PD1	USART8_CK(AF3)/ CAN_TX(AF6)/ FSMC_D3(AF7)	
-	54	83	PD2	I/O	FT	PD2	TIM3_ETR(AF1)/ USART5_RX(AF3)/ USART4_CK(AF4)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							FSMC_NADV(AF7)	
-	-	84	PD3	I/O	FT	PD3	USART2_CTS(AF2)/ USART6_CK(AF3)/ PIOC_IO0(AF4)/ FSMC_CLK(AF7)	
-	-	85	PD4	I/O	FT	PD4	USART2_RTS(AF2)/ USART7_CK(AF3)/ PIOC_IO1(AF4)/ FSMC_NOE(AF7)	
-	-	86	PD5	I/O	FT	PD5	USART2_TX(AF2)/ FSMC_NWE(AF7)	
-	-	87	PD6	I/O	FT	PD6	USART2_RX(AF2)/ FSMC_NWAIT(AF7)	
-	-	88	PD7	I/O	FT	PD7	USART2_CK(AF2)/ FSMC_NE1_NCE2(AF7)	
40	55	89	PB3	I/O/A	-	PB3	CMP1_CHN1/TIM2_CH2(AF1)/ USART5_RX(AF3)/ SPI1_SCK(AF5)	
41	56	90	PB4	I/O	-	PB4	TIM3_CH1(AF1)/ USART5_TX(AF2)/ USART5_CTS(AF3)/ SPI1_MISO(AF5)/ USART1_RTS(AF4)	
42	57	91	PB5	I/O/A	-	PB5	OPA1_CHP0/TIM3_CH2(AF1)/ USART5_RX(AF2)/ USART5_RTS(AF3)/ USART1_CTS(AF4)/ I2C1_SMBA(AF7)/ SPI1_MOSI(AF5)	
44	59	93	PB6	I/O	-	PB6	USBHS_DP/TIM1_CH1(AF0)/ TIM4_CH1(AF1)/ USART1_TX(AF2)/ QSPI_SCSN(AF5)/ I2C1_SCL(AF7)	
43	58	92	PB7	I/O	-	PB7	USBHS_DM/TIM1_CH2(AF0)/ TIM4_CH2(AF1)/	

Pin No.			Pin name	Pin type (1)	I/O structure	Main function after reset	Default alternate function	Remapping function(8)
V205CCT6	V205RCT6	V205VCT6						
							USART1_RX(AF2)/ FSMC_NADV(AF6)/ I2C1_SDA(AF7)	
-	-	94	BOOT0(5)	I	-	BOOT0		
45	60	95	PB8	I/O/A	-	PB8	CMP2_CHP0/TIM1_CH3(AF0)/ TIM4_CH3(AF1)/ USART6_TX(AF2)/ USART4_RTS(AF3)/ CAN_RX(AF6)/ USART6_RTS(AF4)/ I2C1_SCL(AF7)/ QSPI_SIOX0(AF5)	
46	61	96	PB9	I/O	-	PB9	TIM1_BK(AF0)/ TIM4_CH4(AF1)/ USART6_RX(AF2)/ USART4_CTS(AF3)/ USART6_CTS(AF4)/ CAN_TX(AF6)/ QSPI_SIOX1(AF5)/ I2C1_SDA(AF7)	
-	62	97	PE0	I/O	FT	PE0	TIM4_ETR(AF1)/ USART4_TX(AF2)/ USART5_CK(AF3)/ FSMC_NBL0(AF7)	
-	-	98	PE1	I/O	FT	PE1	USART4_RX(AF2)/ FSMC_NBL1(AF7)	
47	63	99	V_{SS_3}	P	-	V_{SS_3}		
-	64	100	V_{IO_3}	P	-	V_{IO_3}		
48	-	-	$V_{DD\_VIO\_3}$	P	-	$V_{DD\_VIO\_3}$		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input; O = CMOS tri-state output;

A = analog signal input or output; P = power; FT = 5V tolerance;

Note 2: I/O pins connect to on-board peripherals/modules via a multiplexer, which permits only one peripheral's application function (AF) to be connected to an I/O pin at a time. This multiplexer utilizes up to 8 multiplex function inputs (AF0 to AF7), configurable via the GPIOx_AFLR and GPIOx_AFHR registers: After reset, the multiplexer defaults to selecting multiplex function 0 (AF0). For further details, refer to the Multiplexed I/O section in the CH32V205RM.

Note 3: Both V_{DD} and V_{BAT} can be connected with an internal analog switch to supply power to the backup area and the pins PC13, PC14 and PC15. This analog switch can only pass a limited current (3mA). When powered by V_{DD}, PC14 and PC15 can be used for GPIO or LSE pins, and PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; PC13, PC14, and PC15 can only operate at frequencies below 2MHz when used as GPIO output pins, with a maximum load capacitance of 30pF. They cannot be used as current sources (e.g., to drive LEDs). When the power is supplied by V_{BAT}, PC14 and PC15 can only be used for LSE pin, and PC13 can be used as TAMPER pin, RTC alarm clock or second output;

Note 4: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32V205RM;

Note 5: Chips without a BOOT0 pin have been internally pulled down to V_{SS}.

Note 6: For the CH32V205CCT6 chip, pins 1 and 2 are default-configured as OSC_IN and OSC_OUT functional pins after chip reset. Software can reconfigure these pins as PD0 and PD1 functional pins. For the CH32V205RCT6 chip, pins 5 and 6 are configured by default as OSC_IN and OSC_OUT functional pins after chip reset. Software can reconfigure these pins as PD0 and PD1 functional pins. However, for the CH32V205VCT6 chip, since PD0 and PD1 are inherently functional pins, no additional software remapping configuration is required. For further details, refer to the Multifunctional I/O section in the CH32V205RM.

Note 7: For the CH32V205CCT6 and CH32V205RCT6 chips, the CAN_RX multiplexing function on PD0 is not available.

Table 2-1-2 CH32V203 pin definitions

Pin No.	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
V203CCT6						
1	V_{BAT}	P	-	V_{BAT}		
2	PC13-TAMPER-RTC (3)	I/O	-	PC13(4)	TAMPER/RTC/TIM1_CH4(AF0)/ I2C2_SCL(AF7)	
3	PC14-OSC32_IN(3)	I/O/A	-	PC14(4)	OSC32_IN/I2C2_SDA(AF7)	
4	PC15-OSC32_OUT(3)	I/O/A		PC15(4)	OSC32_OUT/I2C2_SMBA(AF7)	
5	OSC_IN	I/O/A	-	OSC_IN		PD0(6)
	PD0(6)	I/O	FT	PD0	USART4_CK(AF3)/ CAN_RX(AF6)/	
6	OSC_OUT	I/O/A	-	OSC_OUT		PD1(6)
	PD1(6)	I/O	FT	PD1	USART8_CK(AF3)/	

Pin No. V203CCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
					CAN_TX(AF6)/	
7	NRST	I	-	NRST		
8	V_{SSA}	P	-	V_{SSA}		
9	V_{DDA}	P	-	V_{DDA}		
10	PA0-WKUP	I/O/A	FT	PA0	WKUP/ADC_IN0/ TIM1_ETR(AF0)/ TIM2_CH1_ETR(AF1)/ USART2_CTS(AF2)/ QSPI_SIO2(AF5)	
11	PA1	I/O/A	FT	PA1	ADC_IN1/TIM2_CH2(AF1)/ USART2_RTS(AF2)/ QSPI_SIO3(AF5)	
12	PA2	I/O/A	-	PA2	ADC_IN2/OPA2_OUT2/ CMP1_CHP0/TIM2_CH3(AF1)/ USART2_TX(AF2)/ QSPI_SIO0(AF5)	
13	PA3	I/O/A	-	PA3	ADC_IN3/OPA1_OUT2/ TIM2_CH4(AF1)/ USART2_RX(AF2)/ QSPI_SIO1(AF5)	
14	PA4	I/O/A	-	PA4	ADC_IN4/OPA2_OUT1/ USART2_CK(AF2)/ SPI1_NSS(AF5)	
15	PA5	I/O/A	-	PA5	ADC_IN5/OPA2_CHN1/ USART1_CTS(AF2)/ USART1_CK(AF3)/ USART7_CK(AF4)/ SPI1_SCK(AF5)	
16	PA6	I/O/A	-	PA6	ADC_IN6/OPA1_CHN1/ TIM1_BK(AF0)/ TIM3_CH1(AF1)/ USART1_TX(AF2)/ USART7_TX(AF3)/ USART7_CTS(AF4)/ SPI1_MISO(AF5)	
17	PA7	I/O/A	-	PA7	ADC_IN7/OPA2_CHP1/ TIM1_CH1N(AF0)/	

Pin No. V203CCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
					TIM3_CH2(AF1)/ USART1_RX(AF2)/ USART7_RX(AF3)/ USART7_RTS(AF4)/ SPI1_MOSI(AF5)	
18	PB0	I/O/A	-	PB0	ADC_IN8/OPA1_CHP1/ TIM1_CH2N(AF0)/ TIM3_CH3(AF1)/ USART4_TX(AF2)/ QSPI_SCSN(AF5) USART8_CTS(AF3)/	
19	PB1	I/O/A	-	PB1	ADC_IN9/USART8_RTS(AF3)/ OPA1_OUT1/TIM1_CH3 N(AF0)/ TIM3_CH4(AF1)/ USART4_RX(AF2)/ CMP1_CHN0/QSPI_SCS XN(AF5)	
20	PB2	I/O/A	-	PB2	CMP1_CHP1/USART5_T X(AF3)/ QSPI_SCK(AF5)	
	BOOT1	I	-	BOOT1		
21	PB10	I/O/A	-	PB10	OPA2_CHN0/TIM2_CH3(AF1)/ USART3_TX(AF2)/ QSPI_SIOX2(AF5)/ I2C2_SCL(AF7)	
22	PB11	I/O/A	-	PB11	OPA1_CHN0/CMP2_CHN 1/ TIM2_CH4(AF1)/ USART3_RX(AF2)/ I2C2_SDA(AF7)/ QSPI_SIOX3(AF5)	
23	V_{SS_1}	P	-	V_{SS_1}		
24	$V_{DD\_VIO\_1}$	P	-	$V_{DD\_VIO\_1}$		
25	PB12	I/O/A	-	PB12	OPA1_CHP2/TIM1_BK(A F0)/ CMP1_OUT(AF1)/	

Pin No. V203CCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
					USART3_CK(AF2)/ USART4_CTS(AF3)/ SPI2_NSS(AF5)/ I2C2_SMBA(AF7)	
26	PB13	I/O/A	-	PB13	OPA1_CHNVB/ TIM1_CH1N(AF0)/ USART3_CTS(AF2)/ SPI2_SCK(AF5)	
27	PB14	I/O/A	-	PB14	OPA2_CHP0/TIM1_CH2N (AF0)/ USART3_RTS(AF2)/ SPI2_MISO(AF5)	
28	PB15	I/O/A	-	PB15	OPA2_CHNVB/ TIM1_CH3N(AF0)/ USART1_TX(AF2)/ USART4_RTS(AF3)/ USART6_CK(AF4)/ SPI2_MOSI(AF5)	
29	PA8	I/O/A	-	PA8	CMP2_CHP1/TIM1_CH1(AF0)/ USART1_CK(AF2)/ USART1_RX(AF3)/MCO(AF6)	
30	PA9	I/O/A	-	PA9	CMP2_CHN0/TIM1_CH2(AF0)/ USART1_TX(AF2)/ USART1_RTS(AF3)	
31	PA10	I/O	FT	PA10	TIM1_CH3(AF0)/ USART1_RX(AF2)/ USART1_CK(AF3)	
32	PA11	I/O	FT	PA11	USBFS_DM/TIM1_CH4(AF0)/ USART1_CTS(AF2)/ USART1_TX(AF3)/ CAN_RX(AF6)	
33	PA12	I/O	FT	PA12	USBFS_DP/TIM1_ETR(A F0)/ CMP2_OUT(AF1)/ USART1_RTS(AF2)/	

Pin No. V203CCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
					USART6_TX(AF3)/ QSPI_SCK(AF5)/CAN_TX(AF6)	
34	PA13	I/O	FT	PA13	SWDIO/TIM1_CH1N(AF0)/ TIM2_CH3(AF1)/ USART3_TX(AF2)/ I2C1_SDA(AF7)	
35	V_{SS_2}	P	-	V_{SS_2}		
36	$V_{DD}\_V_{IO\_2}$	P	-	$V_{DD}\_V_{IO\_2}$		
37	PA14	I/O	FT	PA14	SWCLK/TIM1_CH2N(AF0)/ TIM2_CH4(AF1)/ USART8_TX(AF2)/ USART3_RX(AF3)/ USART4_TX(AF4)/ I2C1_SCL(AF7)	
38	PA15	I/O	-	PA15	TIM1_CH3N(AF0)/ TIM2_CH1_ETR(AF1)/ USART8_RX(AF2)/ USART8_CK(AF3)/ USART4_RX(AF4)/ SPI1_NSS(AF5)	
39	PB3	I/O/A	-	PB3	CMP1_CHN1/TIM2_CH2(AF1)/ USART5_RX(AF3)/ SPI1_SCK(AF5)	
40	PB4	I/O	-	PB4	TIM3_CH1(AF1)/ USART5_TX(AF2)/ USART5_CTS(AF3)/ SPI1_MISO(AF5)/ USART1_RTS(AF4)	
41	PB5	I/O/A	-	PB5	OPA1_CHP0/TIM3_CH2(AF1)/ USART5_RX(AF2)/ USART5_RTS(AF3)/ USART1_CTS(AF4)/ I2C1_SMBA(AF7)/	

Pin No. V203CCT6	Pin name	Pin type (1)	I/O structure	Main function (after reset)	Default alternate function	Remapping function(8)
					SPI1_MOSI(AF5)	
42	PB6	I/O	-	PB6	TIM1_CH1(AF0)/ TIM4_CH1(AF1)/ USART1_TX(AF2)/ QSPI_SCSN(AF5)/ I2C1_SCL(AF7)	
43	PB7	I/O	-	PB7	TIM1_CH2(AF0)/ TIM4_CH2(AF1)/ USART1_RX(AF2)/ I2C1_SDA(AF7)	
44	BOOT0(5)	I	-	BOOT0		
45	PB8	I/O/A	-	PB8	CMP2_CHP0/TIM1_CH3(AF0)/ TIM4_CH3(AF1)/ USART6_TX(AF2)/ USART4_RTS(AF3)/ CAN_RX(AF6)/ USART6_RTS(AF4)/ I2C1_SCL(AF7)/ QSPI_SIOX0(AF5)	
46	PB9	I/O	-	PB9	TIM1_BK(AF0)/ TIM4_CH4(AF1)/ USART6_RX(AF2)/ USART4_CTS(AF3)/ USART6_CTS(AF4)/ CAN_TX(AF6)/ QSPI_SIOX1(AF5)/ I2C1_SDA(AF7)	
47	V_{SS_3}	P	-	V_{SS_3}		
48	$V_{DD\_V_{IO\_3}}$	P	-	$V_{DD\_V_{IO\_3}}$		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input; O = CMOS tri-state output;

A = analog signal input or output; P = power; FT = 5V tolerance;

Note 2: I/O pins connect to on-board peripherals/modules via a multiplexer, which permits only one peripheral's application function (AF) to be connected to an I/O pin at a time. This multiplexer utilizes up to 8 multiplex function inputs (AF0 to AF7), configurable via the GPIOx_AFLR and GPIOx_AFHR registers: After reset, the multiplexer defaults to selecting multiplex function 0 (AF0). For further details, refer to the Multiplexed I/O section in the CH32V205RM.

Note 3: Both V_{DD} and V_{BAT} can be connected with an internal analog switch to supply power to the backup area and the pins PC13, PC14 and PC15. This analog switch can only pass a limited current (3mA). When powered by V_{DD}, PC14 and PC15 can be used for GPIO or LSE pins, and PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; PC13, PC14, and PC15 can only operate at frequencies below 2MHz when used as GPIO output pins, with a maximum load capacitance of 30pF. They cannot be used as current sources (e.g., to drive LEDs). When the power is supplied by V_{BAT}, PC14 and PC15 can only be used for LSE pin, and PC13 can be used as TAMPER pin, RTC alarm clock or second output;

Note 4: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32V205RM;

Note 5: Chips without a BOOT0 pin have been internally pulled down to V_{SS}.

Note 6: For the CH32V203CCT6 chip, pins 5 and 6 are configured by default as OSC_IN and OSC_OUT functional pins after chip reset. Software can reconfigure these pins as PD0 and PD1 functional pins. For more details, refer to the Multipurpose I/O section in the CH32V205RM.

2.3 Pin Alternate Functions

Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Note: When pins are configured as multiplexed inputs, optional pins for the same peripheral have priority levels (in the tables below, optional pins within the same row are listed in descending order of priority). When a lower-priority pin is selected as a multiplexed input for a peripheral, higher-priority pins for that same peripheral cannot be simultaneously configured for the same multiplexed function. Example: PA8 (AF0) and PB6 (AF0) are both optional pins for the TIM1_CH1 function, with PA8 having higher priority. If PB6 is used for TIM1_CH1, avoid configuring PA8 as AF0.

Table 2-2-1 ADC pin functions

ADC function	Defaulted pins
ADC_IN0	PA0
ADC_IN1	PA1
ADC_IN2	PA2
ADC_IN3	PA3
ADC_IN4	PA4
ADC_IN5	PA5
ADC_IN6	PA6
ADC_IN7	PA7
ADC_IN8	PB0
ADC_IN9	PB1
ADC_IN10	PC0
ADC_IN11	PC1
ADC_IN12	PC2
ADC_IN13	PC3
ADC_IN14	PC4
ADC_IN15	PC5

Table 2-2-2 TIM pin functions

TIM1 function	Optional pins
TIM1_ETR	PA12(AF0)/PE7(AF0)/PA0(AF0)
TIM1_CH1	PA8(AF0)/PC10(AF0)/PE9(AF0)/PB6(AF0)/PC6(AF0)
TIM1_CH2	PA9(AF0)/PC11(AF0)/PE11(AF0)/PB7(AF0)/PC7(AF0)
TIM1_CH3	PA10(AF0)/PC12(AF0)/PE13(AF0)/PB8(AF0)/PC8(AF0)
TIM1_CH4	PA11(AF0)/PE14(AF0)/PC9(AF0)/PC13(AF0)
TIM1_CH1N	PA7(AF0)/PA13(AF0)/PB13(AF0)/PC3(AF0)/PE8(AF0)

TIM1_CH2N	PA14(AF0)/PB0(AF0)/PB14(AF0)/PC4(AF0)/PE10(AF0)
TIM1_CH3N	PA15(AF0)/PB1(AF0)/PB15(AF0)/PC5(AF0)/PE12(AF0)
TIM1_BK	PA6(AF0)/PB12(AF0)/PE15(AF0)/PB9(AF0)
TIM2 function	Optional pins
TIM2_CH1_ETR	PA0(AF1)/PA15(AF1)
TIM2_CH2	PA1(AF1)/PB3(AF1)
TIM2_CH3	PA2(AF1)/PA13(AF1)/PB10(AF1)
TIM2_CH4	PA3(AF1)/PA14(AF1)/PB11(AF1)
TIM3 function	Optional pins
TIM3_ETR	PD2(AF1)
TIM3_CH1	PA6(AF1)/PB4(AF1)/PC6(AF1)
TIM3_CH2	PA7(AF1)/PB5(AF1)/PC7(AF1)
TIM3_CH3	PB0(AF1)/PC8(AF1)
TIM3_CH4	PB1(AF1)/PC9(AF1)
TIM4 function	Optional pins
TIM4_ETR	PE0(AF1)
TIM4_CH1	PB6(AF1)/PD12(AF1)
TIM4_CH2	PB7(AF1)/PD13(AF1)
TIM4_CH3	PB8(AF1)/PD14(AF1)
TIM4_CH4	PB9(AF1)/PD15(AF1)

Table 2-2-3 I2C pin functions

I2C1 function	Optional pins
I2C1_SCL	PB6(AF7)/PB8(AF7)/PA14(AF7)
I2C1_SDA	PB7(AF7)/PB9(AF7)/PA13(AF7)
I2C1_SMBA	PB5(AF7)
I2C2 function	Optional pins
I2C2_SCL	PB10(AF7)/PC13(AF7)
I2C2_SDA	PB11(AF7)/PC14(AF7)
I2C2_SMBA	PB12(AF7)/PC15(AF7)

Table 2-2-4 SPI pin functions

SPI1 function	Optional pins
SPI1_NSS	PA4(AF5)/PA15(AF5)
SPI1_SCK	PA5(AF5)/PB3(AF5)
SPI1_MOSI	PA7(AF5)/PB5(AF5)
SPI1_MISO	PA6(AF5)/PB4(AF5)

SPI2 function	Optional pins
SPI2_NSS	PB12(AF5)
SPI2_SCK	PB13(AF5)
SPI2_MOSI	PB15(AF5)
SPI2_MISO	PB14(AF5)

Table 2-2-5 USART pin functions

USART1 function	Optional pins
USART1_CK	PA5(AF3)/PA8(AF2)/PA10(AF3)
USART1_RX	PA7(AF2)/PA8(AF3)/PA10(AF2)/PB7(AF2)
USART1_TX	PA6(AF2)/PA9(AF2)/PB6(AF2)/PB15(AF2)/PA11(AF3)
USART1_RTS	PA9(AF3)/PA12(AF2)/PB4(AF4)/PC5(AF2)
USART1_CTS	PA5(AF2)/PA11(AF2)/PB5(AF4)/PC4(AF2)
USART2 function	Optional pins
USART2_CK	PA4(AF2)/PD7(AF2)
USART2_RX	PA3(AF2)/PD6(AF2)
USART2_TX	PA2(AF2)/PD5(AF2)
USART2_RTS	PA1(AF2)/PD4(AF2)
USART2_CTS	PA0(AF2)/PD3(AF2)
USART3 function	Optional pins
USART3_CK	PB12(AF2)/PC12(AF2)/PD10(AF2)
USART3_RX	PA14(AF3)/PB11(AF2)/PC11(AF2)/PD9(AF2)
USART3_TX	PA13(AF2)/PB10(AF2)/PC10(AF2)/PD8(AF2)
USART3_RTS	PB14(AF2)/PD12(AF2)
USART3_CTS	PB13(AF2)/PD11(AF2)
USART4 function	Optional pins
USART4_CK	PD0(AF3)/PD2(AF4)
USART4_RX	PA15(AF4)/PB1(AF2)/PC11(AF3)/PE1(AF2)
USART4_TX	PA14(AF4)/PB0(AF2)/PC10(AF3)/PE0(AF2)
USART4_RTS	PB8(AF3)/PB15(AF3)
USART4_CTS	PB9(AF3)/PB12(AF3)
USART5 function	Optional pins
USART5_CK	PC8(AF4)/PE0(AF3)
USART5_RX	PB5(AF2)/PD2(AF3)/PE9(AF2)/PB3(AF3)
USART5_TX	PB4(AF2)/PC12(AF3)/PE8(AF2)/PB2(AF3)
USART5_RTS	PB5(AF3)
USART5_CTS	PB4(AF3)

USART6 function	Optional pins
USART6_CK	PB15(AF4)/PD3(AF3)
USART6_RX	PB9(AF2)/PC1(AF2)/PE11(AF2)
USART6_TX	PB8(AF2)/PC0(AF2)/PE10(AF2)/PA12(AF3)
USART6_RTS	PB8(AF4)/PC3(AF4)
USART6_CTS	PB9(AF4)/PC2(AF4)
USART7 function	Optional pins
USART7_CK	PA5(AF4)/PD4(AF3)
USART7_RX	PA7(AF3)/PC3(AF2)/PE13(AF2)/PC7(AF4)
USART7_TX	PA6(AF3)/PC2(AF2)/PE12(AF2)/PC6(AF4)
USART7_RTS	PA7(AF4)
USART7_CTS	PA6(AF4)
USART8 function	Optional pins
USART8_CK	PA15(AF3)/PD1(AF3)
USART8_RX	PA15(AF2)/PC5(AF3)/PE15(AF2)/PC12(AF4)
USART8_TX	PA14(AF2)/PC4(AF3)/PE14(AF2)/PC9(AF4)
USART8_RTS	PB1(AF3)
USART8_CTS	PB0(AF3)

Table 2-2-6 CAN pin functions

CAN function	Optional pins
CAN_RX	PA11(AF6)/PB8(AF6)/PD0(AF6)
CAN_TX	PA12(AF6)/PB9(AF6)/PD1(AF6)

Note 7: For the CH32V205CCT6 and CH32V205RCT6 chips, the CAN_RX multiplexing function on PD0 is not available.

Table 2-2-7 Debug pin functions

Debug pin function	Defaulted pins
SWCLK	PA14
SWDIO	PA13

Table 2-2-8 FSMC pin functions

FSMC function	Optional pins
FSMC_D0	PD14(AF7)
FSMC_D1	PD15(AF7)
FSMC_D2	PD0(AF7)
FSMC_D3	PD1(AF7)

FSMC_D4	PE7(AF7)
FSMC_D5	PE8(AF7)
FSMC_D6	PE9(AF7)
FSMC_D7	PE10(AF7)
FSMC_D8	PE11(AF7)
FSMC_D9	PE12(AF7)
FSMC_D10	PE13(AF7)
FSMC_D11	PE14(AF7)
FSMC_D12	PE15(AF7)
FSMC_D13	PD8(AF7)
FSMC_D14	PD9(AF7)
FSMC_D15	PD10(AF7)
FSMC_ADDR16	PD11(AF7)
FSMC_ADDR17	PD12(AF7)
FSMC_ADDR18	PD13(AF7)
FSMC_ADDR19	PE3(AF7)
FSMC_ADDR20	PE4(AF7)
FSMC_ADDR21	PE5(AF7)
FSMC_ADDR22	PE6(AF7)
FSMC_ADDR23	PE2(AF7)
FSMC_NADV	PB7(AF6)/PD2(AF7)
FSMC_CLK	PD3(AF7)
FSMC_NOE	PD4(AF7)
FSMC_NWE	PD5(AF7)
FSMC_NWAIT	PD6(AF7)
FSMC_NE1_NCE2	PD7(AF7)
FSMC_NBL0	PE0(AF7)
FSMC_NBL1	PE1(AF7)

Table 2-2-9 USBPD pin functions

USBPD functions	Optional pins
CC1	PA0(AF7)
CC2	PA1(AF7)

Table 2-2-10 USBFS pin functions

USBFS functions	Defaulted pins
USBFS_DP	PA12
USBFS_DM	PA11

Table 2-2-11 USBHS pin functions

USBHS functions	Defaulted pins
USBHS_DP	PB6
USBHS_DM	PB7

Table 2-2-12 OPA pin functions

OPA1 functions	Optional pins
OPA1_OUT	PB1/OPA1_OUT1, PA3/OPA1_OUT2
OPA1_CHN	PB11/OPA1_CHN0, PA6/OPA1_CHN1
OPA1_CHP	PB5/OPA1_CHP0, PB0/OPA1_CHP1, PB12/OPA1_CHP2
OPA1_CHNVB	PB13
OPA2 functions	Optional pins
OPA2_OUT	PA4/OPA2_OUT1, PA2/OPA2_OUT2
OPA2_CHN	PB10/OPA2_CHN0, PA5/OPA2_CHN1
OPA2_CHP	PB14/OPA2_CHP0, PA7/OPA2_CHP1
OPA2_CHNVB	PB15

Table 2-2-13 CMP pin functions

CMP1 functions	Optional pins
CMP1_CHP	PA2/CMP1_CHP0, PB2/CMP1_CHP1
CMP1_CHN	PB1/CMP1_CHN0, PB3/CMP1_CHN1
CMP1_OUT	PB12(AF1)
CMP2 functions	Optional pins
CMP2_CHP	PB8/CMP2_CHP0, PA8/CMP2_CHP1
CMP2_CHN	PA9/CMP2_CHN0, PB11/CMP2_CHN1
CMP2_OUT	PA12(AF1)

Table 2-2-14 QSPI pin functions

QSPI functions	Optional pins
QSPI_SCK	PA12(AF5)/PB2(AF5)
QSPI_SCSN	PB0(AF5)/PB6(AF5)
QSPI_SIO0	PA2(AF5)/PC9(AF5)/PD11(AF5)
QSPI_SIO1	PA3(AF5)/PC10(AF5)/PD12(AF5)
QSPI_SIO2	PA0(AF5)/PE6(AF5)
QSPI_SIO3	PA1(AF5)/PD13(AF5)
QSPI_SCSXN	PB1(AF5)/PC11(AF5)

QSPI_SIOX0	PB8(AF5)/PE7(AF5)
QSPI_SIOX1	PB9(AF5)/PE8(AF5)
QSPI_SIOX2	PB10(AF5)/PE9(AF5)
QSPI_SIOX3	PB11(AF5)/PE10(AF5)

Table 2-2-15 MCO pin functions

MCO functions	Optional pins
MCO	PA8(AF6)

Table 2-2-16 PIOC pin functions

PIOC functions	Optional pins
PIOC_IO0	PA11(AF4)/PB10(AF4)/PD3(AF4)/PE3(AF4)
PIOC_IO1	PA12(AF4)/PB11(AF4)/PD4(AF4)/PE4(AF4)

Chapter 3 Electrical Characteristics

3.1 Test Conditions

Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency.

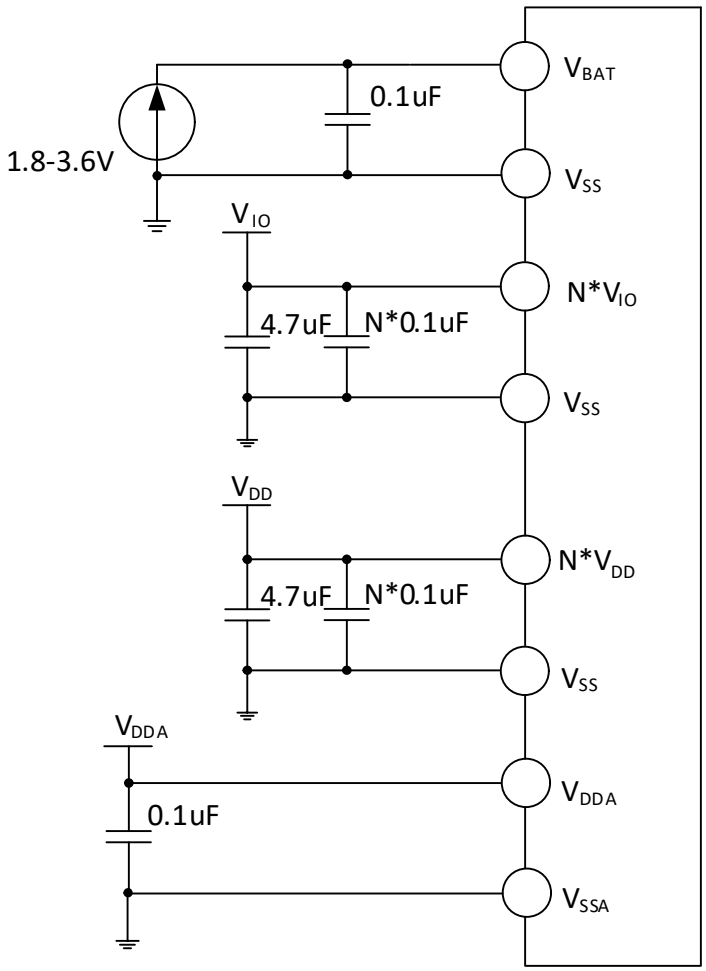
The typical values for the CH32V205 are provided for design guidance based on an ambient temperature of 25℃ and an operating environment where $V_{DD} = V_{DDA} = V_{IO} = 3.3V$.

The typical values for the CH32V203 are provided for design guidance based on an ambient temperature of 25℃ and an operating environment where $V_{DD\_IO} = V_{DDA} = 3.3V$.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1-1 CH32V205 standard power supply typical circuit



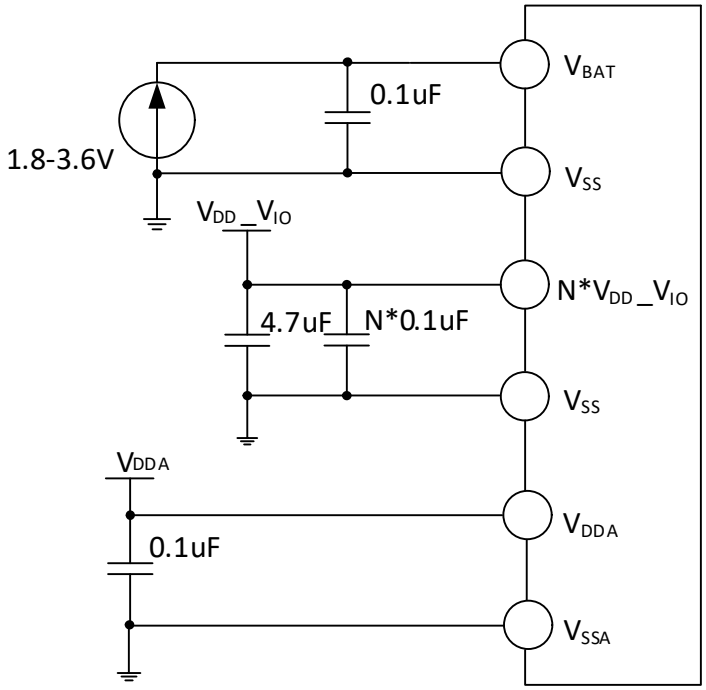
Note:

In certain chip packages, V_{DD} and V_{IO} may have multiple pins. Power pins with the same designation must be shorted.

Each V_{DD} pin should be externally connected to a 0.1uF decoupling capacitor. It is recommended to add a 4.7uF decoupling capacitor in parallel across the entire V_{DD} power supply.

Each V_{IO} pin should be externally connected to a 0.1uF decoupling capacitor. It is recommended to add a 4.7uF decoupling capacitor in parallel across the entire V_{IO} power supply.

Figure 3-1-2 CH32V203 standard power supply typical circuit



Note:

In certain chip packages, $V_{DD}\_V_{IO}$ may have multiple pins. All pins sharing this designation must be shorted together.

Each $V_{DD}\_V_{IO}$ pin requires an external 0.1uF decoupling capacitor. Additionally, a 4.7uF decoupling capacitor should be connected in parallel across the entire $V_{DD}\_V_{IO}$ power supply.

3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{BAT} V_{REF+}, V_{IO})	-0.3	4.0	V
V_{IN}	Input voltage on the FT (5V tolerance) pin	V_{SS}-0.3	5.5	V
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	V
$\|\Delta V_{DD\_x}\|$	Variations between different main power supply pins		20	mV

$\|\triangle V_{SS\_x}\|$	Variations between different ground pins		20	mV
$V_{ESD(HBM)}$	ESD Electrostatic Discharge Voltage (HBM) on normal I/O Pins	4K		V
	ESD Electrostatic Discharge Voltage (HBM) on USB Pins	4K		V
I_{VDD}	Total current into $V_{DD}/V_{DDA}/V_{I/O}$ power lines (source)		250	mA
I_{Vss}	Total current out of V_{SS} ground lines (sink)		250	mA
I_{IO}	Sink current on any I/O and control pin		25	mA
	Output current on any I/O and control pin		-25	mA
$I_{INJ(PIN)}$	Injected current on NRST pin		±5	mA
	Injected current on HSE's OSC_IN pin and LSE's OSC_IN pin		±5	mA
	Injected current on other pins		±5	mA
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		±25	mA

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 4-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	Standard operating voltage	Unused USB	1.8	3.6	V
		Use USB	3.15	3.45	
V_{DDA}	Analog operating voltage ($V_{DDA} = V_{DD}$)	When the ADC is not in use, V_{DDA} must not fall below V_{IO}.	1.8	3.6	V
		When using ADC or enabling TKEY, V_{DDA} must not be lower than V_{IO}, and V_{REF+} must not exceed V_{DDA}.	2.4	3.6	V
		When using an OPA, the op-amp output must not exceed V_{IO}.	1.8	3.6	V
V_{BAT}(1)	Backup operating voltage	Cannot exceed V_{DD}	1.8	3.6	V
V_{IO}	Output voltage of most I/O pins	VIO cannot exceed VDD	1.45	3.6	V
V_{REF+}(3)	Positive reference voltage of ADC module	V_{REF+} cannot exceed V_{DDA}	1.8	3.6	V
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	105	℃

Note:

1. Keep the wiring from the battery to V_{BAT} as short as possible.

2. Voltage relationships: $V_{DD} \geq V_{DDA} \geq V_{IO}$; and $V_{DDA} \geq V_{REF+}$.

3. The reference voltage V_{REF+} must not exceed V_{DDA}. ADC performance degrades when V_{REF+} falls below 2.4V.

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit

t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		50	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Programmable voltage detector level selection	PLS[2:0] = 000 (rising edge)		1.73		V
		PLS[2:0] = 000 (falling edge)		1.68		V
		PLS[2:0] = 001 (rising edge)		1.91		V
		PLS[2:0] = 001 (falling edge)		1.85		V
		PLS[2:0] = 010 (rising edge)		2.11		V
		PLS[2:0] = 010 (falling edge)		2.05		V
		PLS[2:0] = 011 (rising edge)		2.32		V
		PLS[2:0] = 011 (falling edge)		2.25		V
		PLS[2:0] = 100 (rising edge)		2.51		V
		PLS[2:0] = 100 (falling edge)		2.43		V
		PLS[2:0] = 101 (rising edge)		2.68		V
		PLS[2:0] = 101 (falling edge)		2.60		V
		PLS[2:0] = 110 (rising edge)		2.89		V
		PLS[2:0] = 110 (falling edge)		2.79		V
		PLS[2:0] = 111 (rising edge)		3.07		V
		PLS[2:0] = 111 (falling edge)		2.97		V
$V_{PVDhyst}$(1)	PVD hysteresis		0.05	0.08	0.14	V
$V_{POR/PDR}$(2)	Power-on/power-down reset threshold	Rising edge	1.34	1.56	1.78	V
		Falling edge	1.32	1.54	1.76	V
$V_{PDRhyst}$(2)	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		5	6.5	30	mS

Note: 1. Design parameters;

2. Normal temperature test value.

3.3.3 Embedded Reference Voltage

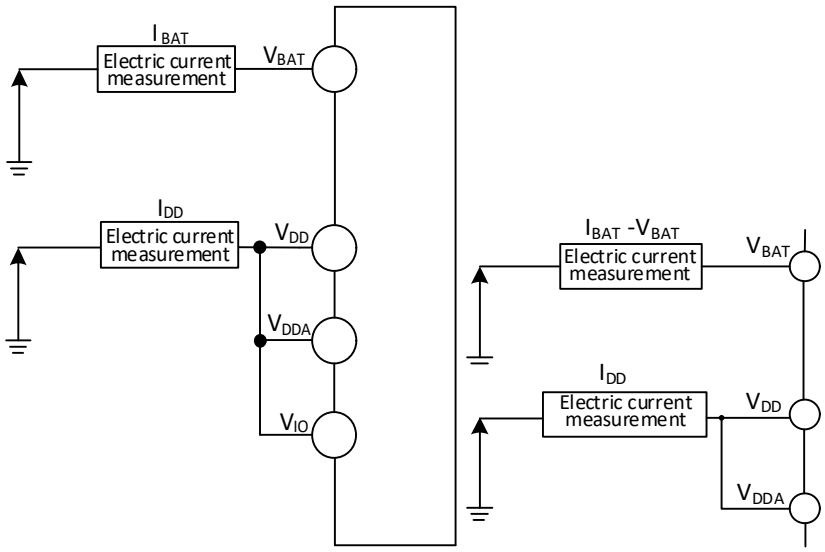
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40℃~85℃	1.19	1.22	1.25	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling is recommended.			20	us

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2-1 CH32V205 Current consumption measurement

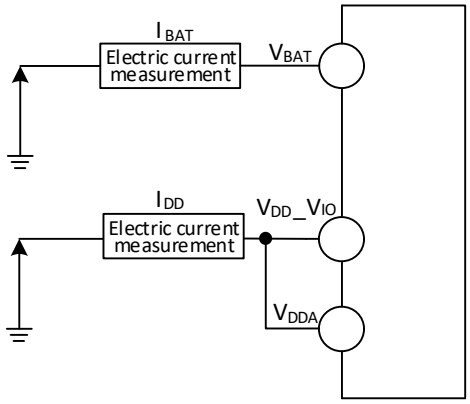


CH32V205 is in the following conditions:

At normal temperature with V_{DD} = V_{DDA} = V_{IO} = 3.3V, during testing: All I/O pins are configured as pull-down inputs, operating at the high-speed internal RC oscillator HSI (HSI = 8M). F_{PLCK1} = F_{HCLK}/2 and F_{PLCK2} = F_{HCLK}. Power consumption when enabling or disabling all peripheral clocks.

Note: For pins that are not packaged in small package models or are packaged but unused, it is recommended to configure them as pull-up inputs or pull-down inputs. Failure to do so may affect current specifications. For specific procedures, please refer to the EVT low-power example code.

Figure 3-2-2 CH32V203 Current consumption measurement



CH32V203 is in the following conditions:

At normal temperature with V_{DD_IO} = V_{DDA} = 3.3V, during testing: All I/O pins are configured as pull-down inputs, operating at the high-speed internal RC oscillator HSI (HSI = 8M). F_{PLCK1} = F_{HCLK}/2 and F_{PLCK2} = F_{HCLK}. Power consumption when enabling or disabling all peripheral clocks.

Table 3-6 The data processing code is run from FLASH, LDOTRIM[1:0]=10b (default value) and LDO_EC=0

Symbol	Parameter	Condition			Typ.		Unit
		HSILP	PLLON	F_{HCLK}	All peripherals	All peripherals	

					enabled	disabled	
I_{DD}(1)	Supply current in Run mode	0	1	192MHz	21.4	12.6	mA
		0	1	160MHz	19.8	11.1	
		0	1	96MHz	11.5	7.1	
		0	0	8MHz	2.1	1.7	
		1	0	1MHz	1.3	1.2	
	Supply current in Sleep mode(At this time, peripheral power supply and clock hold are maintained)	0	1	192MHz	13.8	5.1	mA
		0	1	160MHz	13.4	4.6	
		0	1	96MHz	7.7	3.3	
		0	0	8MHz	1.9	1.5	
		1	0	1MHz	1.2	1.1	

Note: The above are measured parameters.

Table 3-7 The data processing code is run from FLASH, FLASH enters low-power mode, LDOTRIM[1:0]= 01b, LDO_EC=0

Symbol	Parameter	Condition			Typ.		Unit
		HSILP	PLLON	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(2)	Supply current in Run mode	0	1	192MHz	20.3	11.3	mA
		0	1	160MHz	19.3	11.1	
		0	1	96MHz	10.6	6.4	
		0	0	8MHz	1.1	0.7	
		1	0	1MHz	0.2	0.2	
	Supply current in Sleep mode(At this time, peripheral power supply and clock hold are maintained)	0	1	192MHz	11.5	3.8	mA
		0	1	160MHz	11.2	3.3	
		0	1	96MHz	6.3	2.2	
		0	0	8MHz	0.8	0.4	
		1	0	1MHz	0.2	0.2	

Note: 1. When FLASH_LP_REG=1 and FLASH_LP[11:10]=10b, the FLASH enters low-power mode.

2. The above are measured parameters.

Table 3-8-1 The data processing code runs from FLASH, and the typical current consumption in stop and standby modes

Symbol	Parameter	Condition								Typ.	Unit
		HIS, HSE LSI, LSE	RAMLV	R28KSTY	R4KSTY	LDO_EC	LPDS	PDDS	LDO		
I_{DD}(1)	Supply current in STOP mode 1(2)	All disabled	X	X	X	0	0	0	10	275	uA
	Supply current in STOP mode 2(2)	All disabled	X	X	X	1	0	0	10	265	
	Supply current in STOP mode 3	All disabled	0	X	X	X	1	0	X	117	
	Supply current in STOP mode 4	All disabled	1	X	X	X	1	0	X	115	
	Supply current in STANDBY mode	Only enable LSI	0	1	1	X	X	1	X	24	uA
		All disabled	0	1	1	X	X	1	X	23.8	
		All disabled	1	1	1	X	X	1	X	14.3	
		Only enable LSI	1	0	1	X	X	1	X	7.2	
		All disabled	1	0	1	X	X	1	X	7.0	
		Only enable LSI	X	0	0	X	X	1	X	3.7	
		All disabled	X	0	0	X	X	1	X	3.5	
I_{DD_VBAT}(1)	Supply current for the backup area (remove V_{DD} and V_{DDA}, power only via V_{BAT})	Only enable LSE	X	0	0	X	X	1	X	1.8	uA
		All disabled	X	0	0	X	X	1	X	1.5	

Note: 1. The above are measured parameters.

2. Set FLASH_LP[11:10]=10.

Table 3-8-2 The data processing code runs from SRAM, and the typical current consumption in Stop modes

Symbol	Parameter	Condition								Typ.	Unit
		HIS, HSE LSI, LSE	RAMLV	R28KSTY	R4KSTY	LDO_EC	LPDS	PDDS	LDO		
I_{DD}(1)	Supply current in STOP mode 1(2)	All disabled	X	X	X	0	0	0	01	272	uA
	Supply current in	All	X	X	X	1	0	0	01	262	

	STOP mode 2(2)	disabled									

Note: 1. The above are measured parameters.

2. Set FLASH_LP[11:10]=10.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		3	8	25	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		0.8*V_{DD}		V_{DD}	V
V_{HSEL}(1)	OSC_IN input pin low-level voltage		0		0.2*V_{DD}	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

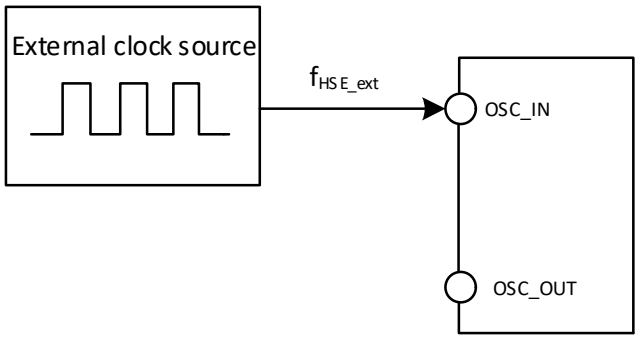


Table 3-10 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.8V_{DD}		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		0		0.2V_{DD}	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current				±1	uA

Figure 3-4 External low-frequency clock source circuit

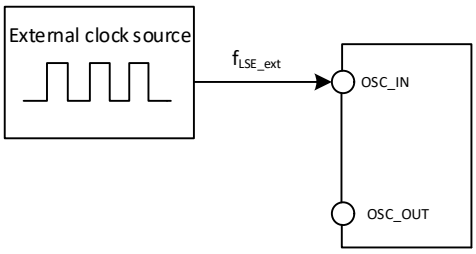


Table 3-11 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		3	8	25	MHz
R_F	Feedback resistance			250		kΩ
C	Recommended load capacitance and corresponding crystal series impedance R_S	R_S=60Ω(1)		20		pF
I_2	HSE drive current	V_{DD} = 3.3V, 20p load		1		mA
		Low power mode, V_{DD} = 3.3V, 20p load		0.55		
g_m	Oscillator transconductance	Startup		21		mA/V
$t_{SU(HSE)}$	Startup time(2)	V_{DD} is stable		1.5	4.5	ms

Note 1: It is recommended that the crystal's ESR does not exceed 80Ω. Prioritize crystals with lower ESR values. Refer to the crystal manual for load capacitance requirements.

2. Start time refers to the time difference from HSEON being activated until HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1}=C_{L2}.

Figure 3-5 Typical circuit of external 8M crystal

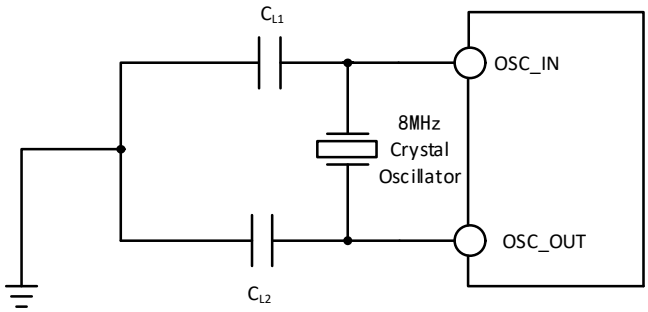


Table 3-12 Low-speed external clock generated by generated from a crystal/ceramic resonator (f_{LSE}=32.768KHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback resistance			5		MΩ
C	Recommended load capacitance and corresponding crystal serial impedance R_S	R_S=70kΩ			15	pF
i_2	LSE drive current	V_{DD} = 3.3V		0.36		uA
g_m	Oscillator transconductance	Startup		26		uA/V
$t_{SU(LSE)}$	Startup time	V_{DD} is stable		1000		mS

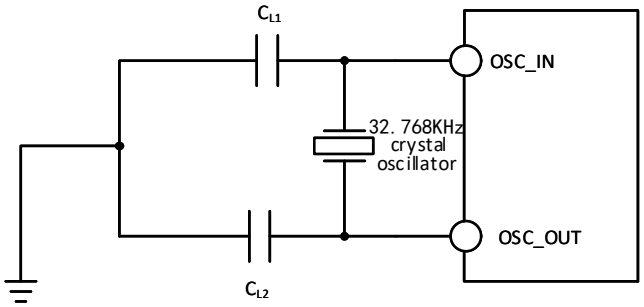
Note 1: The startup time refers to the time difference between the moment LSEON is activated and the moment LSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, usually

C_{L1}=C_{L2}, which is about 12pF.

Figure 3-6 Typical circuit of external 32.768K crystal



Note: The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$. C_{stray} is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF.

3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			8		MHz
		Low power mode		1		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	T_A = 0℃~70℃	-0.7		0.7	%
		T_A = -40℃~85℃	-1		1	%
		Low-power mode	-5		5	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time				8	us
$I_{DD(HSI)}$	HSI oscillator power consumption			200		uA
		Low power mode		24		uA

Table 3-14 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		30	40	50	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time			400		us
$I_{DD(LSI)}$	LSI oscillator power consumption			240		nA

3.3.7 PLL Characteristics

Table 3-15 PLL characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		3	8	25	MHz
	PLL input clock duty		40		60	%

	cycle					
F_{PLL_OUT}	PLL multiplier output clock		24		208(1)	MHz
t_{LOCK}	PLL lock time			80	200	us
$I_{DD(PLL)}$	PLL power consumption	Input frequency: 8 MHz Output frequency: 192 MHz		0.2		mA

Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.

3.3.8 Wakeup Time from Low-power Mode

Table 3-16 Wakeup time from low-power mode

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	0.2	us
t_{wustop}	Wakeup from Stop mode	Wake up using HSI RC clock	15	us
$t_{WUSTDBY}$	Wakeup from Standby mode	Wake up using HSI RC clock	90	us

Note: The above are measured parameters.

3.3.9 Memory Characteristics

Table 3-17 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) programming time		1.6	2.0	2.5	ms
t_{erase_page}	Page (256 bytes) erase time		5.0	6.2	7.3	ms
t_{erase_sec}	Sector (2K bytes) erase time		5.0	6.3	7.5	ms

Table 3-18 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25℃	300K			Times
		T_A = 85℃	100K			Times
t_{RET}	Data retention	T_A = 25℃	20			Years
		T_A = 85℃	10			Years

3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.41*V_*+0.53		V_*+0.3	V
		V_* = 3.3V	1.9		3.6	
	FT I/O pin, input high level voltage		0.40*V_*+0.55		5.0	V
		V_* = 3.3V	1.9		5.0	
	BOOT0 pin, input high level voltage		0.84*V_*-0.04		V_*+0.3	V
		V_* = 3.3V	2.7		3.6	

V_{IL}	Standard I/O pin, input low level voltage		-0.3		0.32*V∗-0.16	V
		V∗ = 3.3V	-0.3		0.9	
	FT I/O pin, input low level voltage		-0.3		0.31*V∗-0.15	V
		V∗ = 3.3V	-0.3		0.9	
	BOOT0 pin, input low level voltage		-0.3		0.79*V∗-0.60	V
		V∗ = 3.3V	-0.3		2.0	
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis			220		mV
	FT I/O pin Schmitt trigger voltage hysteresis			200		mV
	BOOT0 Schmitt trigger voltage hysteresis			200		mV
I_{lkg}	Standard I/O pin input leakage current				1	uA
	FT I/O pin input leakage current				3	uA
	BOOT0 pin input leakage current				1	uA
R_{PU}	Pull-up equivalent resistance		30	40	55	kΩ
R_{PD}	Pull-down equivalent resistance		30	40	55	kΩ
C_{IO}	I/O pin capacitance			5		pF

Note: I/O pins are powered by V_{IO}, V_{DD}, or V_{BAT}. In the table above, V∗ may represent V_{IO}, V_{DD}, or V_{BAT} depending on the specific pin.

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±10mA current, In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-20-1 Output voltage characteristics (Excluding pins PC13 to PC15)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 8 pins are sunk	TTL port, I_{IO} = +15mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V≤ V∗ ≤3.6V	V∗-0.4		
V_{OL}	Output low level when 8 pins are sunk	CMOS port, I_{IO} = +15mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V≤ V∗ ≤3.6V	V∗-0.4		
V_{OL}	Output low level when 8 pins are sunk	I_{IO} = +10mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	1.8V≤ V∗ ≤3.6V	V∗-0.4		
V_{OL}	Output low level when 8 pins are sunk	I_{IO} = +10mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	1.8V≤ V∗ ≤3.6V	V∗-0.4		

Note: 1. In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

2. In the table above, V∗ may be represented as V_{IO} or V_{DD} depending on the specific pin.

Table 3-20-2 Output voltage characteristics (Refer to pins PC13 to PC15)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 3 pins are sunk	I_{IO} = +5mA 2.7V≤ V∗ ≤3.6V		0.4	V
V_{OH}	Output high level when 3 pins are sourced	I_{IO} = +1.5mA 2.7V≤ V∗ ≤3.6V	V∗-0.4		
V_{OL}	Output low level when 3 pins are sunk	I_{IO} = +3mA 1.8V≤ V∗ ≤3.6V		0.4	V
V_{OH}	Output high level when 3 pins are sourced	I_{IO} = +1mA 1.8V≤ V∗ ≤3.6V	V∗-0.4		

Note: In the table above, V∗ may be represented as V_{DD} or V_{BAT} depending on the specific pin.

Table 3-21 Output AC characteristics (Excluding pins PC13 to PC15)

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10	$F_{max(IO)out}$	Maximum frequency	CL = 50pF, V∗ = 2.7-3.6V		16	MHz
			CL = 50pF, V∗ = 1.8-2.7V		8	MHz
			CL = 30pF, V∗ = 2.7-3.6V		18	MHz
			CL = 30pF, V∗ = 1.8-2.7V		9	MHz
			CL = 10pF, V∗ = 2.7-3.6V		20	MHz
			CL = 10pF, V∗ = 1.8-2.7V		10	MHz
	$t_{r(IO)out}$/ $t_{f(IO)out}$	Output high to low fall time	CL = 50pF, V∗ = 2.7-3.6V		14	ns
			CL = 50pF, V∗ = 1.8-2.7V		24	ns
			CL = 30pF, V∗ = 2.7-3.6V		12	ns
			CL = 30pF, V∗ = 1.8-2.7V		21	ns
			CL = 10pF, V∗ = 2.7-3.6V		10	ns
			CL = 10pF, V∗ = 1.8-2.7V		18	ns
01	$F_{max(IO)out}$	Maximum frequency	CL = 50pF, V∗ = 2.7-3.6V		50	MHz
			CL = 50pF, V∗ = 1.8-2.7V		25	MHz
			CL = 30pF, V∗ = 2.7-3.6V		65	MHz
			CL = 30pF, V∗ = 1.8-2.7V		27	MHz
			CL = 10pF, V∗ = 2.7-3.6V		85	MHz
			CL = 10pF, V∗ = 1.8-2.7V		30	MHz
	$t_{r(IO)out}$/ $t_{f(IO)out}$	Output high to low fall time	CL = 50pF, V∗ = 2.7-3.6V		5.6	ns
			CL = 50pF, V∗ = 1.8-2.7V		8.8	ns
			CL = 30pF, V∗ = 2.7-3.6V		4.3	ns
			CL = 30pF, V∗ = 1.8-2.7V		6.8	ns
			CL = 10pF, V∗ = 2.7-3.6V		3.0	ns
			CL = 10pF, V∗ = 1.8-2.7V		4.8	ns
11	$F_{max(IO)out}$	Maximum frequency	CL = 50pF, V∗ = 2.7-3.6V		60	MHz
			CL = 50pF, V∗ = 1.8-2.7V		38	MHz

			CL = 30pF, V∗ = 2.7-3.6V		100	MHz
			CL = 30pF, V∗ = 1.8-2.7V		50	MHz
			CL = 10pF, V∗ = 2.7-3.6V		140	MHz
			CL = 10pF, V∗ = 1.8-2.7V		70	MHz
	$t_{r(IO)out}$/ $t_{f(IO)out}$	Output high to low fall time	CL = 50pF, V∗ = 2.7-3.6V		4.6	ns
			CL = 50pF, V∗ = 1.8-2.7V		7.4	ns
			CL = 30pF, V∗ = 2.7-3.6V		3.3	ns
			CL = 30pF, V∗ = 1.8-2.7V		4.3	ns
			CL = 10pF, V∗ = 2.7-3.6V		2.0	ns
			CL = 10pF, V∗ = 1.8-2.7V		3.3	ns

Note: 1. In the table above, V∗ may be represented as V_{IO} or V_{DD} depending on the specific pin.

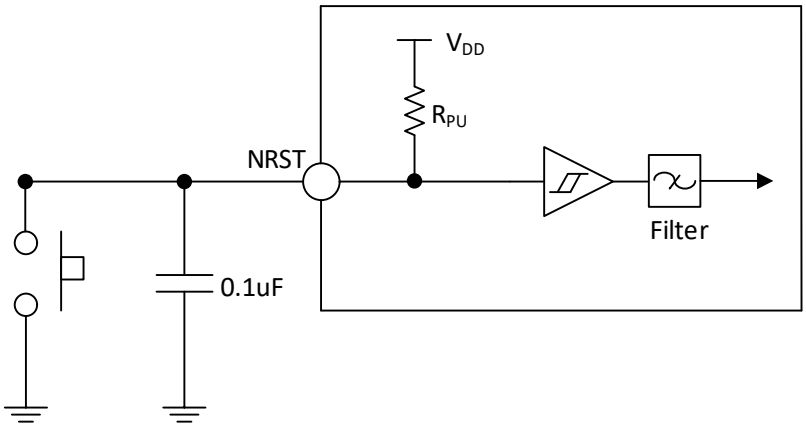
2. The USB interface I/O complies only with the parameters specified in MODEx[1:0]=10b.

3. When functioning as GPIO output pins, PC13, PC14, and PC15 operate at frequencies below 2MHz with a maximum load capacitance of 30pF.

3.3.11 NRST Pin Characteristics

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin



Note: The capacitor shown in the diagram is optional and can be used to filter out key bounce.

Table 3-22 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		-0.3		0.32*V_{IO}-0.16	V
$V_{IH(NRST)}$	NRST input high-level voltage		0.41*V_{IO}+0.53		V_{IO}+0.3	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis			220		mV
R_{PU}(1)	Pull-up equivalent resistance		30	40	50	kΩ
$V_{F(NRST)}$	NRST input filtered pulse width				100	ns
$V_{NF(NRST)}$	NRST input not filtered		300			ns

	pulse width					

Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).

3.3.12 USB PD Interface Characteristics

Table 3-23-1 PD interface I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{Rise}	Rising time	The time between 10% and 90% of the range, with the minimum value being the time under no-load conditions.	300	400		ns
t_{Fall}	Falling time	The time between 10% and 90% of the range, with the minimum value being the time under no-load conditions.	300	400		ns
V_{Swing}	Output voltage swing (Peak-to-peak)		1.04	1.12	1.20	V
Z_{Driver}	Output impedance		26		90	Ω

Table 3-23-2 Type-C I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CCIL}(1)	CC pin input low voltage	HVT = 0, FT I/O input	0		0.8	V
		HVT = 1, high threshold detection input	0		2.0	
V_{CCIH}(1)	CC pin input high voltage	HVT = 0, FT I/O input	2.0		V_{IO}	V
		HVT = 1, high threshold detection input	2.45		V_{IO}	
V_{CChys}	Hysteresis voltage	HVT = 0, FT I/O input	90			mV
		HVT = 1, high threshold detection input		120		
I_{pu}	Pull-up current	PAD < V_{IO}-0.6V		80		uA
				180		uA
				330		uA

Note: 1. The V_{CCIL} and V_{CCIH} values corresponding to HVT=1 are design parameters.

3.3.13 TIM Timer Characteristics

Table 3-24-1 TIM1/2/3 characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz	5.21		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 192MHz	0	96	MHz
R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz	0.0052	341	us
t_{MAX_COUNT}	Maximum possible count			65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz		22.4	s

Table 3-24-2 TIM4 characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz	5.21		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 192MHz	0	96	MHz
R_{esTIM}	Timer resolution			32	bit
$t_{COUNTER}$	32-bit counter clock cycle when the internal clock is selected		1	2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz	0.0052	$2^{32}/192$	us
t_{MAX_COUNT}	Maximum possible count			2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 192MHz		$2^{32}*2^{32}/192$	us

3.3.14 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram

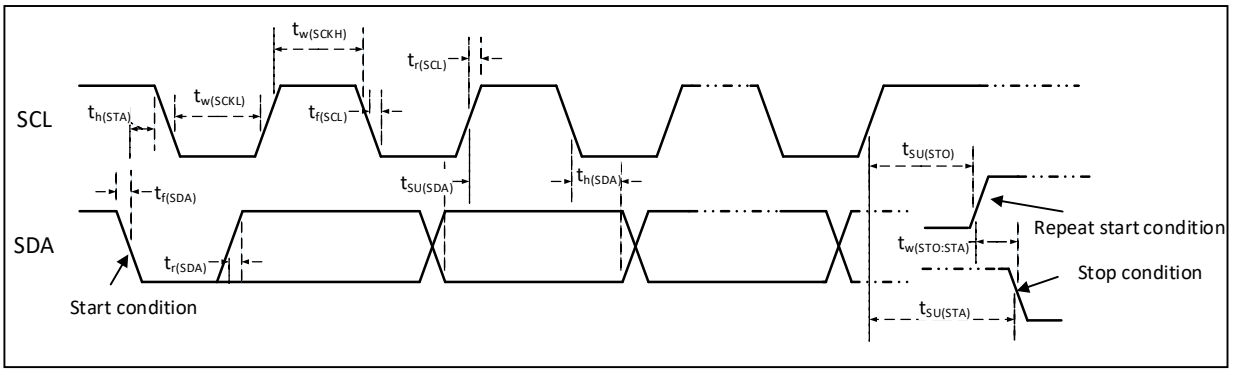


Table 3-25 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.15 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode

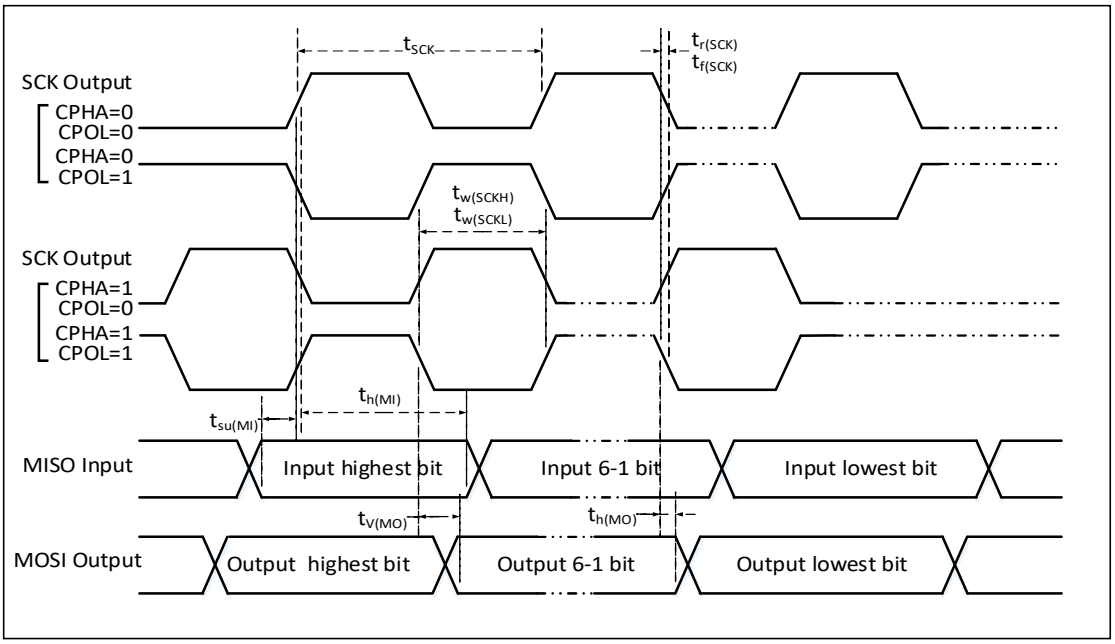


Figure 3-10-1 SPI timing diagram in Slave mode (CPHA=0, CPOL=0)

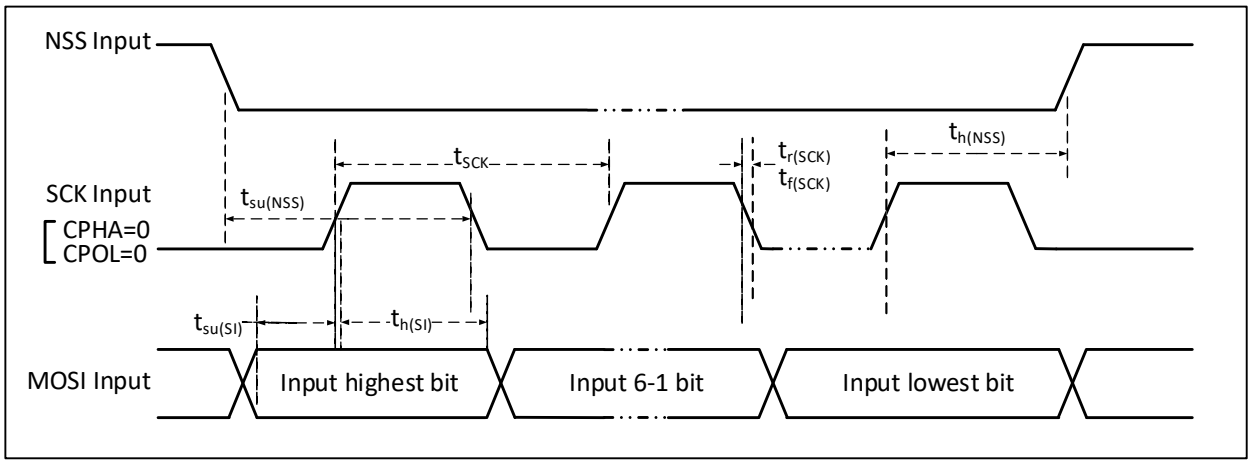


Figure 3-10-2 SPI timing diagram in Slave mode (CPHA=0, CPOL=1)

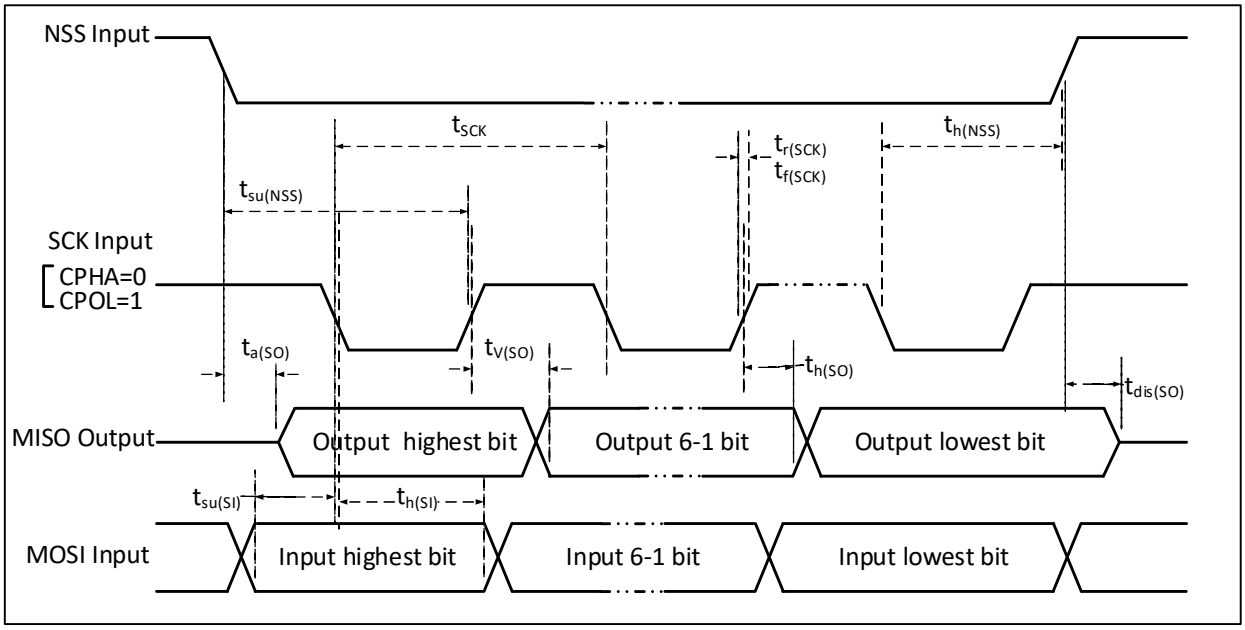


Figure 3-11-1 SPI timing diagram in Slave mode (CPHA=1, CPOL=0)

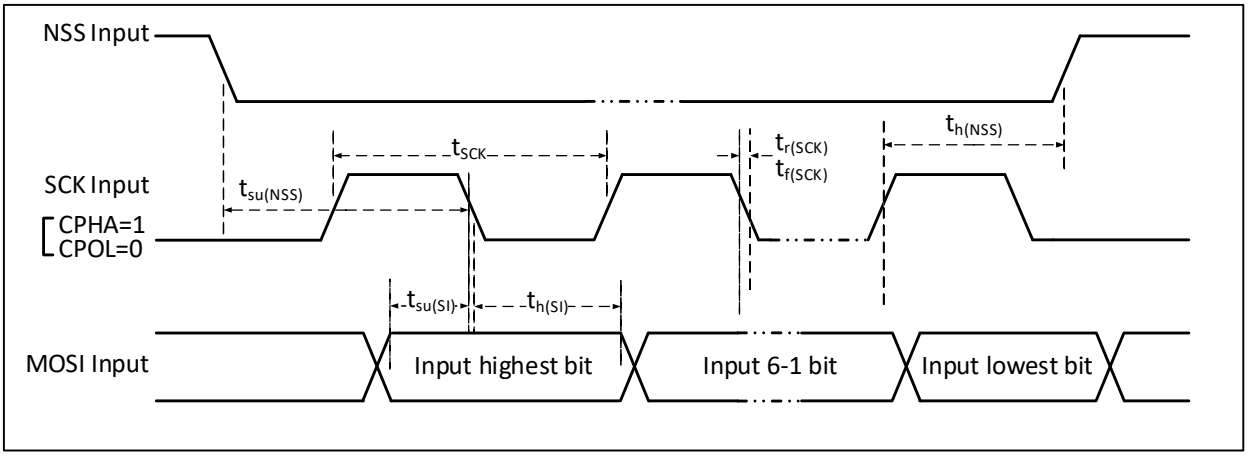


Figure 3-11-2 SPI timing diagram in Slave mode (CPHA=1, CPOL=1)

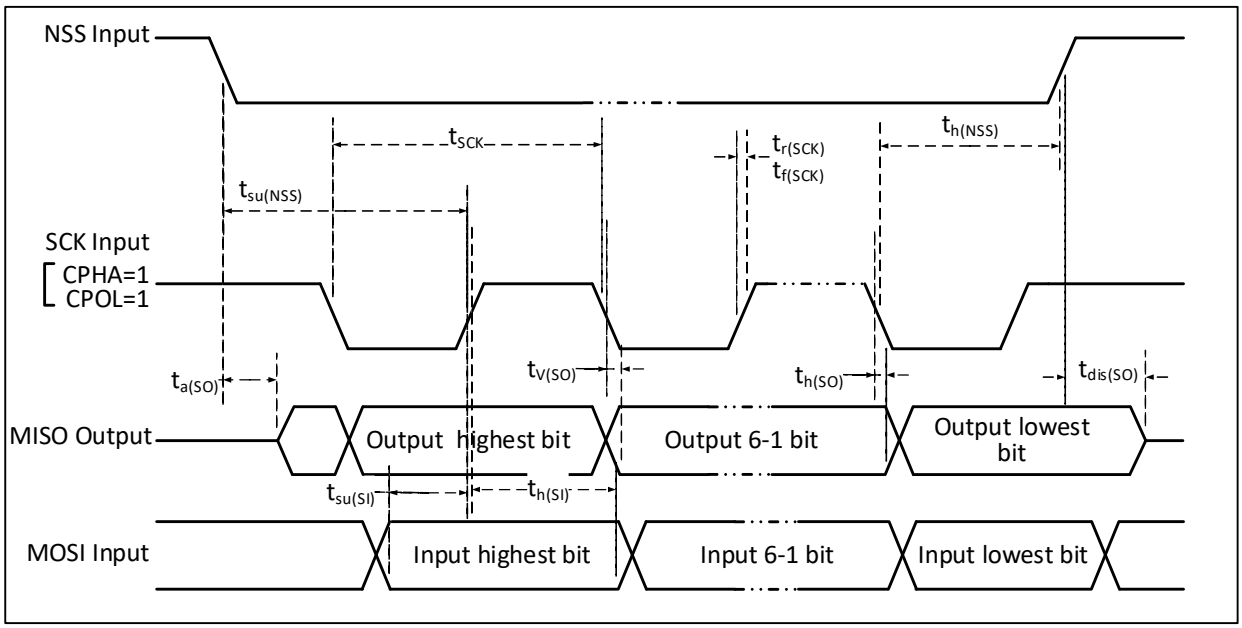


Table 3-26 SPI interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode			96	MHz
		Slave mode			96	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF			8	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode		$2*t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode		$2*t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 24MHz, Prescaler factor = 4		70	97	ns
$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	15		ns
		Master mode	HSRXEN = 1	$15-0.5*t_{SCK}$		
$t_{SU(SI)}$		Slave mode		4		ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	4		ns
		Master mode	HSRXEN = 1	$0.5*t_{SCK}-4$		
$t_{h(SI)}$		Slave mode		4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	$1*t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			15	ns
$t_{V(MO)}$		Master mode (After enable edge)			5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)		8		ns
$t_{h(MO)}$		Master mode (After enable edge)		0		ns

3.3.16 USB Interface Characteristics

Table 3-27 USB I/O characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	USB operating voltage		3.15		3.45	V
V_{SE}	Single-ended receiver threshold	V_{DD} = 3.3V	1.2		1.9	V
V_{OL}	Static output low level				0.3	V
V_{OH}	Static output high level		2.8		3.6	V
V_{HSSQ}	High-speed suppression information detection threshold		100		150	mV
V_{HSDSC}	High-speed disconnection detection threshold		500		625	mV
V_{HSOI}	High-speed idle level		-10		10	mV
V_{HSOH}	High-speed data high level		360		440	mV
V_{HSOL}	High-speed data low level		-10		10	mV
V_{BC_REF}	BC CMP reference voltage			0.4		V
V_{BC_SRC}	BC protocol output voltage			0.6		V

3.3.17 12-bit ADC Characteristics

Table 3-28 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
V_{REF+}(2)(3)	Positive reference voltage	$V_{REF+} \leq V_{DDA}$, no less than 2.4V is recommended.	1.8		V_{DDA}	V
I_{DDA}	V_{DDA} supply current			700		uA
I_{REFP}	V_{REF+} supply current			175		uA
f_{ADC}	ADC clock frequency			16	64	MHz
f_S	Sampling rate			1	4	MHz
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
R_{ADC}	Sampling switch resistance			0.2		kΩ
R_{AIN}	External input impedance	For details, refer to Formula 1.			50	kΩ
C_{ADC}	Internal sample and hold capacitor			10.3		pF
t_{CAL}	Calibration time			36		$1/f_{ADC}$
t_{Iat}	Injected trigger conversion latency				2	$1/f_{ADC}$
t_{Iatr}	Regular trigger conversion latency				2	$1/f_{ADC}$
t_{STAB}	Sampling time				1	us
t_s	Power-on time	f_{ADC} = 80MHz	3.5		239.5	$1/f_{ADC}$
		f_{ADC} = 96MHz	5.5		239.5	

t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80MHz	16		252	$1/f_{ADC}$
		f_{ADC} = 96MHz	18		252	

Note: 1. All above are design parameters.

2. The reference voltage V_{REF+} must not exceed V_{DDA}. ADC performance degrades when V_{REF+} falls below 2.4V.

3. The external capacitor for V_{REF+} must be placed as close as possible to the pin to avoid affecting ADC performance.

Formula 1: Maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above Formula 1 is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 3-29 Maximum R_{AIN} when f_{ADC} = 80MHz

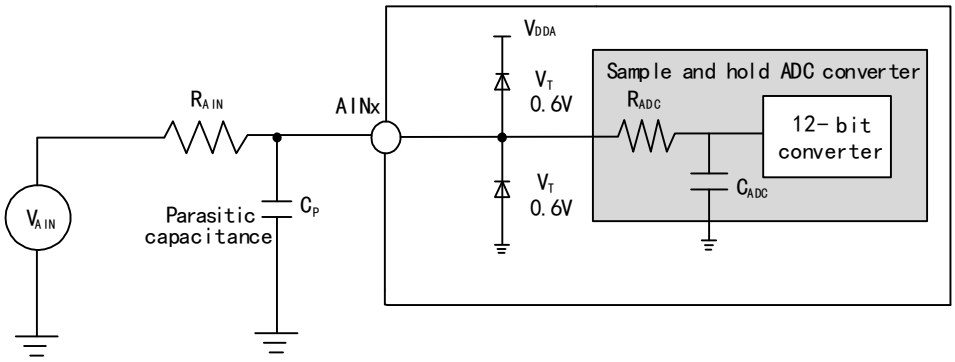
T_S(cycle)	t_S (us)	Maximum R_{AIN}(kΩ)
3.5	0.044	0.24
5.5	0.069	0.49
7.5	0.094	0.74
11.5	0.144	1.25
13.5	0.169	1.49
28.5	0.356	3.39
41.5	0.519	5.02
239.5	2.994	29.93

Table 3-30 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
E0	Offset error	f_{ADC} = 80MHz,		±3	±8	LSB
ED	Differential nonlinearity error	R_{AIN} < 1kΩ,		±3	±6	
EL	Integral nonlinearity error	V_{DDA} = 3.3V		±3	±6	
E0	Offset error	f_{ADC} = 96MHz,		±6	±11	
ED	Differential nonlinearity error	R_{AIN} < 0.5kΩ,		±3	±8	
EL	Integral nonlinearity error	V_{DDA} = 3.3V		±6	±10	

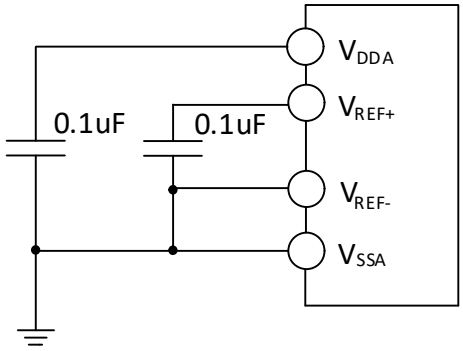
Note: All above are design parameters.

Figure 3-12 ADC typical connection diagram



C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-13 Analog power supply and decoupling circuit reference



3.3.18 Temperature Sensor Characteristics

Table 3-31 Temperature sensor characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{TS}	Measurement range of temperature sensor		-40		85	℃
A_{TSC}	Measurement range of temperature sensor after software calibration			±12		℃
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.8	mV/℃
V_{25}	Voltage at 25℃		1.35	1.43	1.5	V
T_{S_temp}	ADC sampling time when reading temperature	f_{ADC} = 8MHz			20	us

3.3.19 OPA Characteristics

Table 3-32-1 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	No less than 2V is	1.8	3.3	3.6	V

		recommended.				
V_{CM}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage (OPA1)	After calibration		±0.2		mV
	Input offset voltage (OPA2)	After calibration		±0.9		mV
I_{LOAD}	Drive current	R_{LOAD} = 4kΩ			900	uA
I_{LOAD_PGA}	PGA mode drive current				500	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		550		uA
CMRR(1)	Common mode rejection ratio	@1kHz		115		dB
PSRR(1)	Power supply rejection ratio	@1kHz		81		dB
Av(1)	Open loop gain	C_{LOAD} = 5pF		115		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		14		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		75		°
S_R(1)	Slew rate limited	C_{LOAD} = 5pF	10	12	14	V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DDA}/2, C_{LOAD} = 50pF, R_{LOAD} = 4kΩ		0.2		us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ	V_{DDA}-100	V_{DDA}-60		mV
		R_{LOAD} = 20kΩ	V_{DDA}-100	V_{DDA}-60		
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ		3	10	mV
		R_{LOAD} = 20kΩ		3	10	
PGA Gain(1)	Internal in-phase PGA	Gain = 4, V_{INP} <(V_{DDA}/3) (OPA2)	-1		1	%
		Gain = 8, V_{INP} <(V_{DDA}/7) (OPA1&OPA2)	-1		1	%
		Gain = 16, V_{INP} <(V_{DDA}/15) (OPA1&OPA2)	-1		1	%
		Gain = 32, V_{INP} <(V_{DDA}/31) (OPA1&OPA2)	-1		1	%
		Gain = 64, V_{INP} <(V_{DDA}/63) (OPA1)	-2		2	%
V_B	Recommended DC bias voltage in PGA mode	PGADIF = 1	0.2	V_{DDA}/2	V_{DDA}-0.2	V
Delta R	Absolute value change of resistance		-15		15	%
eN(1)	Equivalent input noise; Disable chopper	R_{LOAD} = 4kΩ@1kHz		105		nV/ sqrt(Hz)
		R_{LOAD} = 20kΩ@1KHz		105		
	Equivalent input noise; Enable chopper@1MHz	R_{LOAD} = 4kΩ@1kHz		28		
		R_{LOAD} =		28		

	(OPA1)	20kΩ@1KHz				

Note:

1. Design parameters;

2. Load current will limit the saturated output voltage;

3. OPA output voltage shall not exceed V_{IO}.

Table 3-32-2 OPA characteristics (High-speed mode)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage	No less than 2V is recommended.	1.8	3.3	3.6	V
V_{CM}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage (OPA1)			±4		mV
	Input offset voltage (OPA2)			±4		mV
I_{LOAD}	Drive current	R_{LOAD} = 4kΩ			900	uA
I_{LOAD_PGA}	PGA mode drive current				500	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		1250		uA
CMRR(1)	Common mode rejection ratio	@1kHz		90		dB
PSRR(1)	Power supply rejection ratio	@1kHz		81		dB
Av(1)	Open loop gain	C_{LOAD} = 5pF		105		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		25		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		80		°
S_R(1)	Slew rate limited	C_{LOAD} = 5pF	30	45	53	V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DDA}/2, C_{LOAD} = 50pF, R_{LOAD} = 4kΩ		0.15		us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ	V_{DDA}-80	V_{DDA}-55		mV
		R_{LOAD} = 20kΩ	V_{DDA}-80	V_{DDA}-55		
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ		3	10	mV
		R_{LOAD} = 20kΩ		3	10	
PGA Gain(1)	Internal in-phase PGA	Gain = 4, V_{INP} <(V_{DDA}/3) (OPA2)	-1		1	%
		Gain = 8, V_{INP} <(V_{DDA}/7) (OPA1&OPA2)	-1		1	%
		Gain = 16, V_{INP} <(V_{DDA}/15) (OPA1&OPA2)	-1		1	%
		Gain = 32, V_{INP} <(V_{DDA}/31) (OPA1&OPA2)	-1		1	%
		Gain = 64, V_{INP} <(V_{DDA}/63) (OPA1)	-2		2	%

V_B	Recommended DC bias voltage in PGA mode	PGADIF = 1	0.2	$V_{DDA}/2$	V_{DDA}-0.2	V
Delta R	Absolute value change of resistance		-15		15	%
eN(1)	Equivalent input noise; Disable chopper	R_{LOAD} = 4kΩ@1kHz		73		nV/ sqrt(Hz)
		R_{LOAD} = 20kΩ@1KHz		73		
	Equivalent input noise; Enable chopper@1MHz (OPA1)	R_{LOAD} = 4kΩ@1kHz		13		
		R_{LOAD} = 20kΩ@1KHz		13		

Note:

1. Design parameters;

2. Load current will limit the saturated output voltage;

3. OPA output voltage shall not exceed V_{IO}.

3.3.20 CMP Characteristics

Table 3-33-1 CMP characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		1.8	3.3	3.6	V
V_{CM}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$(1)	Input offset voltage			±1.4		mV
I_{DDCMP}	Current consumption			100		uA
V_{hys}(1)	Hysteresis voltage	HYS[1:0] = 00		0		mV
		HYS[1:0] = 01		±12.5		
		HYS[1:0] = 10		±25		
		HYS[1:0] = 11		±50		
t_D(1)	Comparator delay. V_{INP} varies from (V_{INN}-100mV) to (V_{INN}+100mV) change	0≤ V_{INN}≤ V_{DDA}		15		ns

Note: 1. Design parameters are guaranteed.

Table 3-33-2 CMP characteristics (low-power mode)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		1.8	3.3	3.6	V
V_{CM}	Common mode input voltage		0		V_{DDA}	V
$V_{IOFFSET}$(1)	Input offset voltage			±1.5		mV
I_{DDCMP}	Current consumption			40		uA
V_{hys}(1)	Hysteresis voltage	HYS[1:0] = 00		0		mV
		HYS[1:0] = 01		±10		
		HYS[1:0] = 10		±20		
		HYS[1:0] = 11		±40		
t_D(1)	Comparator delay. V_{INP} varies from (V_{INN}-100mV)	0≤ V_{INN}≤ V_{DDA}		25		ns

	to (V_{INN}+100mV) change					

Note: 1. Design parameters are guaranteed.

3.3.21 FSMC Characteristics

Figure 3-14 Asynchronous bus multiplexing PSRAM/NOR read operation waveform

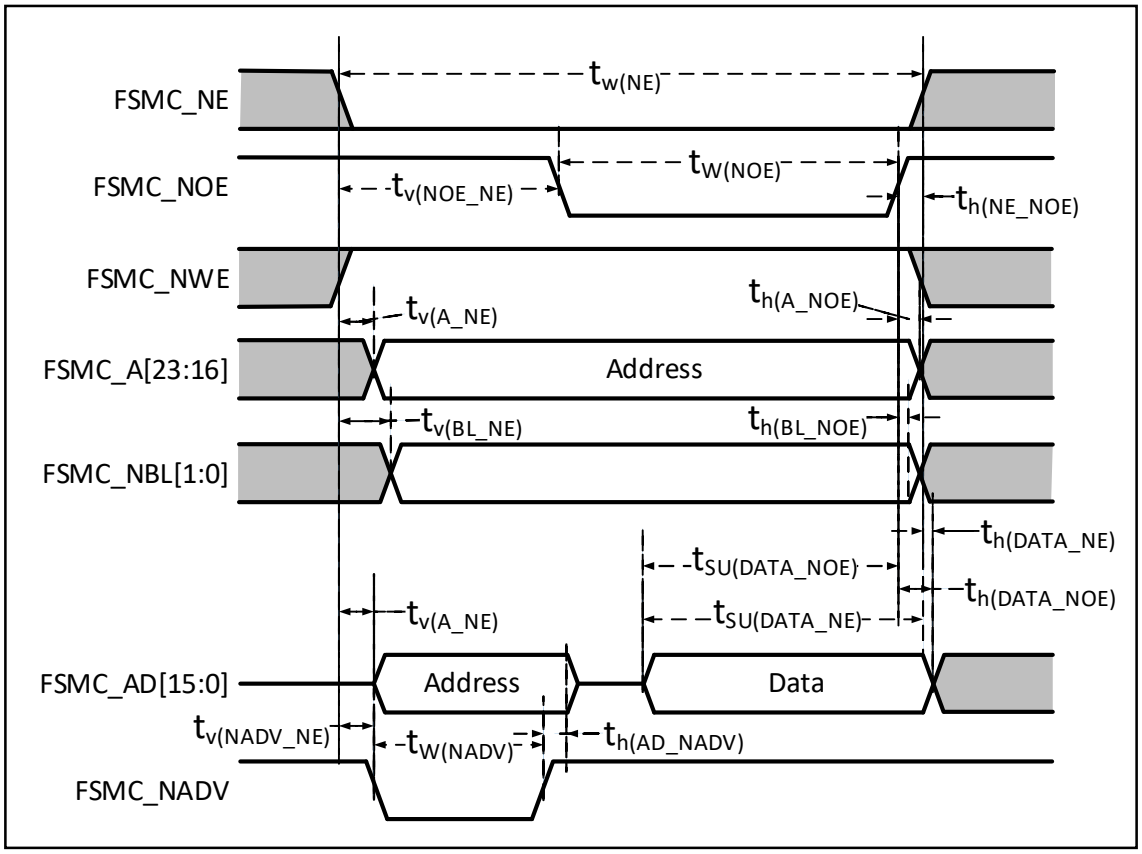


Table 3-34 Timing of PSRAM/NOR read operation for asynchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_{W\ (NE)}$	FSMC_NE low level time	7*t_{HCLK}		ns
$t_{V\ (NOE\_NE)}$	FSMC_NE low to FSMC_NOE low	0		
$t_{W\ (NOE)}$	FSMC_NOE low time	7*t_{HCLK}		
$t_{h\ (NE\_NOE)}$	Retention time from FSMC_NOE high to FSMC_NE high	0		
$t_{V\ (A\_NE)}$	FSMC_NE low to FSMC_A active	0	5	
$t_{V\ (NADV\_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W\ (NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h\ (AD\_NADV)}$	Effective retention time of FSMC_AD (address) after FSMC_NADV is high.	2*t_{HCLK}		
$t_{h\ (A\_NOE)}$	Address retention time after FSMC_NOE is high	0		
$t_{h\ (BL\_NOE)}$	FSMC_BL holding time after FSMC_NOE is high.	0		
$t_{V\ (BL\_NE)}$	FSMC_NE low to FSMC_BL active	0	5	
$t_{SU\ (DATA\_NE)}$	Setup time from data to FSMC_NE high	3*t_{HCLK}		
$t_{SU\ (DATA\_NOE)}$	Setup time from data to FSMC_NOE high	3*t_{HCLK}		
$t_{h\ (DATA\_NE)}$	Data retention time after FSMC_NE is high	0		

$t_{h\ (DATA\_NOE)}$	Data retention time after FSMC_NOE is high	0		

Figure 3-15 Asynchronous bus multiplexing PSRAM/NOR write operation waveform

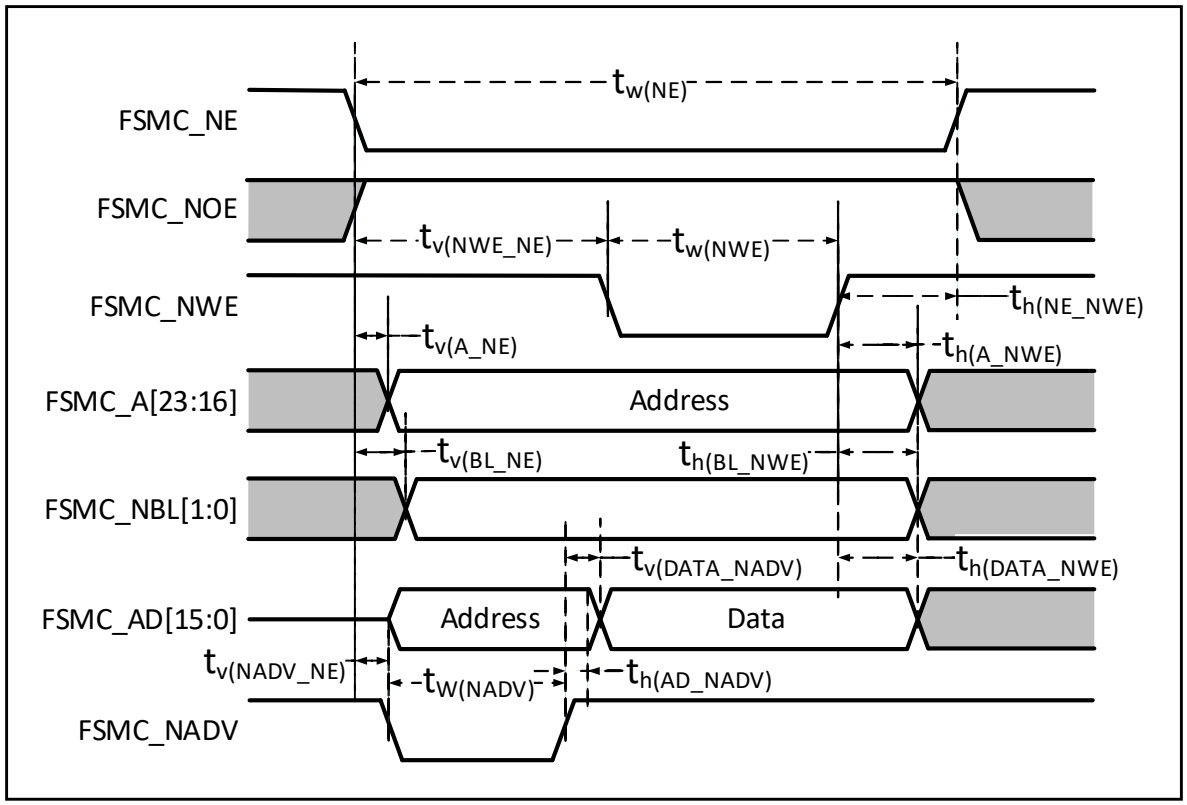


Table 3-35 Timing of PSRAM/NOR write operation for asynchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_{W\ (NE)}$	FSMC_NE low level time	$5*t_{HCLK}$		ns
$t_{V\ (NEW\_NE)}$	FSMC_NE low to FSMC_NWE low	$3*t_{HCLK}$		
$t_{W\ (NWE)}$	FSMC_NWE low time	$2*t_{HCLK}$		
$t_{h\ (NE\_NWE)}$	Retention time from FSMC_NWE high to FSMC_NE high	t_{HCLK}		
$t_{V\ (A\_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{V\ (NADV\_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W\ (NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h\ (AD\_NADV)}$	Effective retention time of FSMC_AD (address) after FSMC_NADV is high.	$2*t_{HCLK}$		
$t_{h\ (A\_NWE)}$	Address retention time after FSMC_NWE is high	t_{HCLK}		
$t_{V\ (BL\_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{h\ (BL\_NWE)}$	FSMC_BL retention time after FSMC_NWE is high	t_{HCLK}		
$t_{V\ (DATA\_NADV)}$	FSMC_NADV high to data retention time	$2*t_{HCLK}$		
$t_{h\ (DATA\_NWE)}$	Data retention time after FSMC_NWE is high	t_{HCLK}		

Figure 3-16 Synchronous bus multiplexing NOR/PSRAM read waveform

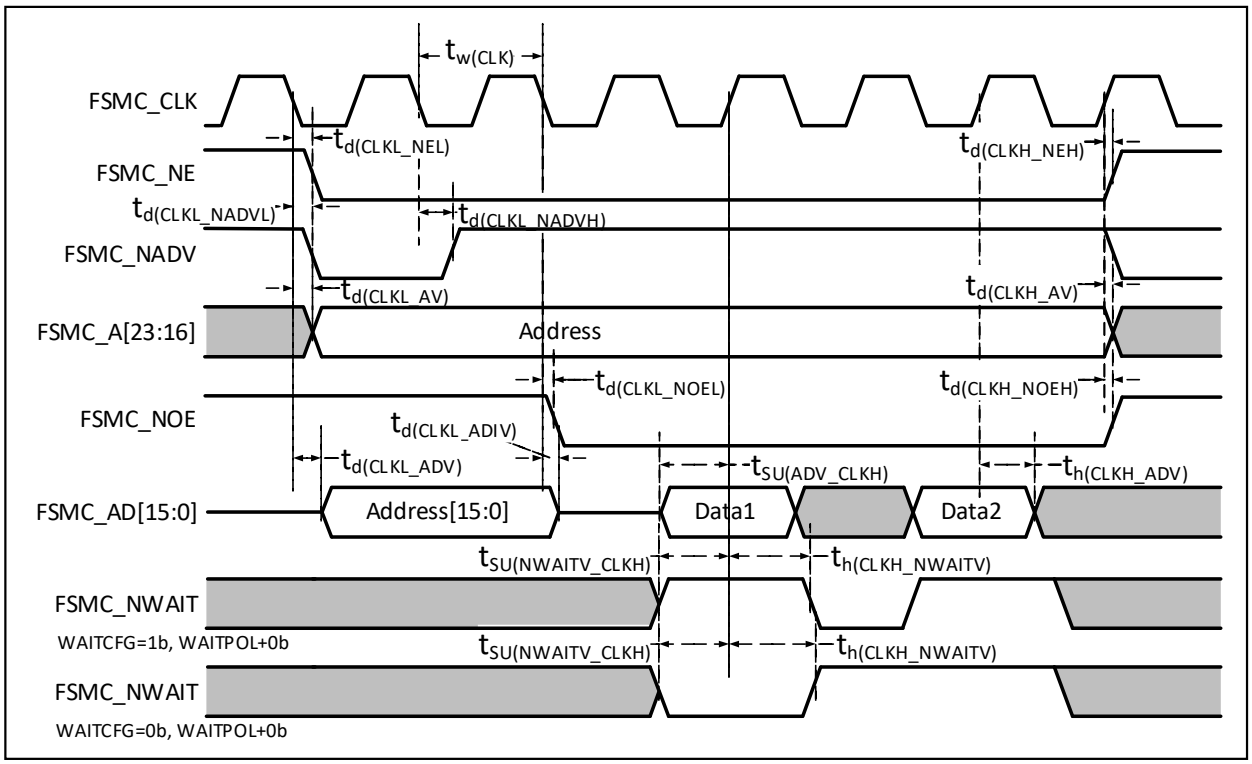


Table 3-36 Timing of NOR/PSRAM read operation for synchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_{W\ (CLK)}$	FSMC_CLK cycle	$2*t_{HCLK}$		ns
$t_{d\ (CLKL\_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d\ (CLKH\_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5*t_{HCLK}$	$0.5*t_{HCLK}$	
$t_{d\ (CLKL\_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d\ (CLKL\_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d\ (CLKL\_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d\ (CLKH\_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d\ (CLKL\_NOEL)}$	FSMC_CLK low to FSMC_NOE low	$2*t_{HCLK}$		
$t_{d\ (CLKH\_NOEH)}$	FSMC_CLK high to FSMC_NOE high	t_{HCLK}		
$t_{d\ (CLKL\_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d\ (CLKL\_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{SU\ (ADV\_CLKH)}$	FSMC_CLK high before FSMC_AD[15:0] valid data	8		
$t_{h\ (CLKH\_ADV)}$	FSMC_CLK high after FSMC_AD[15:0] valid data	8		
$t_{SU\ (NWAITV\_CLKH)}$	FSMC_CLK high before FSMC_NWAIT valid	6		
$t_{h\ (CLKH\_NWAITV)}$	FSMC_CLK high after FSMC_NWAIT valid	2		

Figure 3-17 Synchronous bus multiplexing PSRAM write waveform

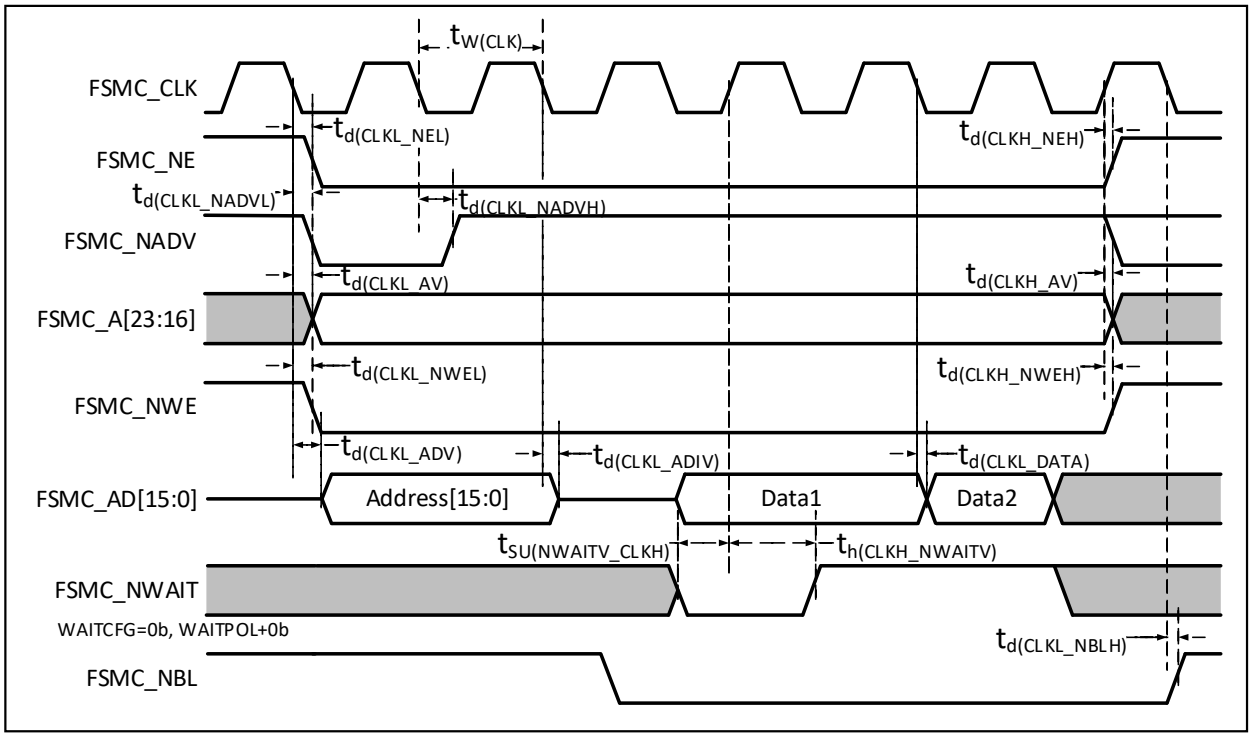


Table 3-37 Timing of NOR/PSRAM read operation for synchronous bus multiplexing

Symbol	Parameter	Min.	Max.	Unit
$t_{W(CLK)}$	FSMC_CLK cycle	$2*t_{HCLK}$		ns
$t_{d(CLKL\_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d(CLKH\_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5*t_{HCLK}$	$0.5*t_{HCLK}$	
$t_{d(CLKL\_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d(CLKL\_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d(CLKL\_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d(CLKH\_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d(CLKL\_NWEL)}$	FSMC_CLK low to FSMC_NWE low	0		
$t_{d(CLKH\_NWEH)}$	FSMC_CLK high to FSMC_NWE high	0		
$t_{d(CLKL\_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d(CLKL\_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{d(CLKL\_DATA)}$	FSMC_CLK low after FSMC_AD[15:0] valid	2		
$t_{SU(NWAITV\_CLKH)}$	FSMC_CLK high before FSMC_NWAIT valid	6		
$t_{h(CLKH\_NWAITV)}$	FSMC_CLK high after FSMC_NWAIT valid	2		
$t_{d(CLKL\_NBLH)}$	FSMC_CLK low to FSMC_NBL high	2		

Waveform and timing of NAND controller

Test conditions: NAND operation mode, 16-bit data width selected, ECC calculation circuit enabled, 512-byte page size. Other timing configurations set via configuration registers: FSMC_PCR2=0x0002005E, FSMC_PMEM2=0x01020301, FSMC_PATT2=0x01020301.

Figure 3-18 NAND controller read operation waveform

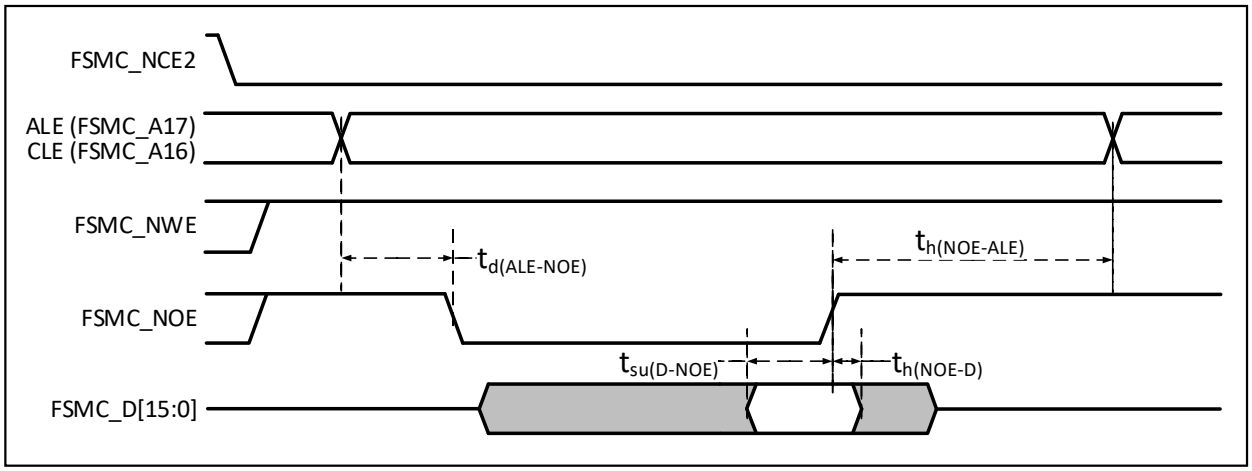


Figure 3-19 NAND controller write operation waveform

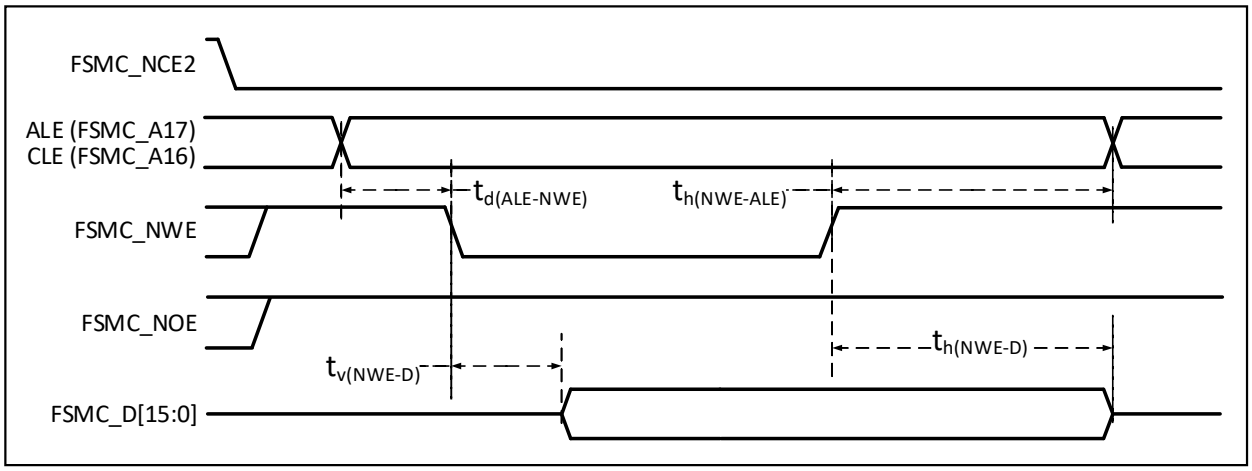


Figure 3-20 Read operation waveform of NAND controller in general storage space

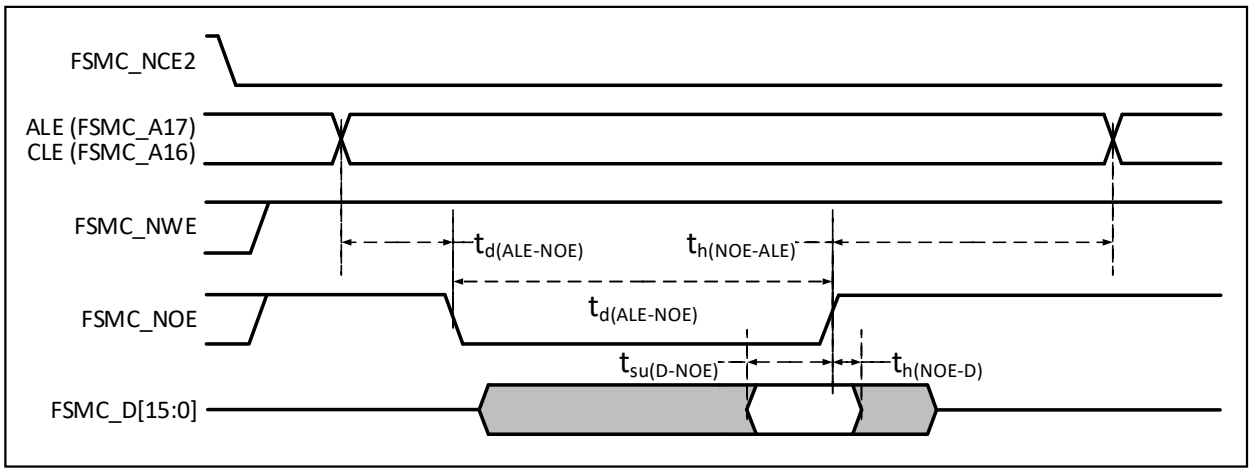


Figure 3-21 Write operation waveform of NAND controller in general storage space

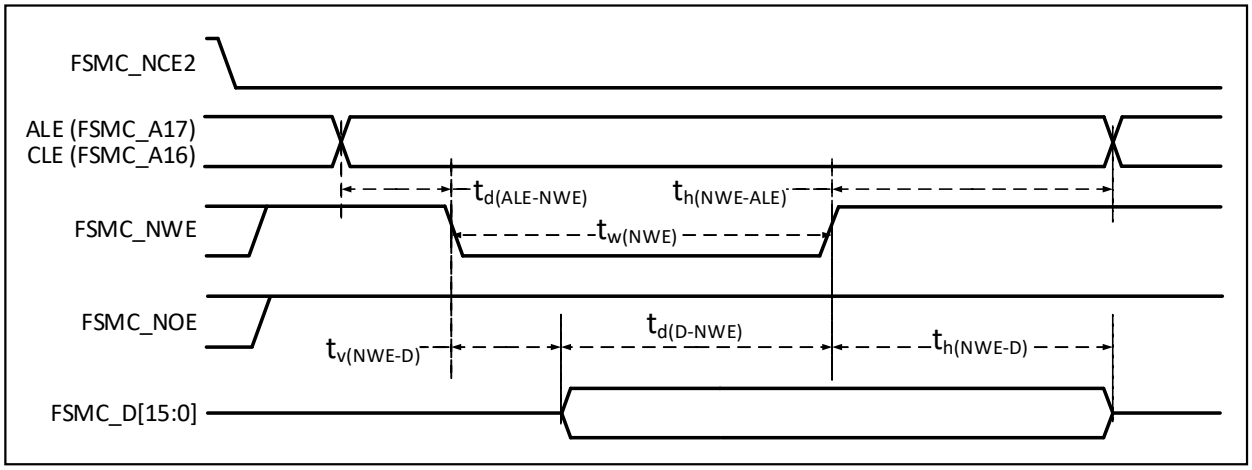


Table 3-38 Timing characteristics of read/write cycle of NAND Flash memory

Symbol	Parameter	Min.	Max.	Unit
$t_{d\ (D\text{-}NWE)}$	FSMC_NWE high before FSMC_D[15:0] data is valid	$4*t_{HCLK}$		ns
$t_{w\ (NOE)}$	FSMC_NOE low time	$4*t_{HCLK}$		
$t_{su\ (D\text{-}NOE)}$	FSMC_NOE high before FSMC_D[15:0] data is valid	20		
$t_{h\ (NOE\text{-}D)}$	FSMC_NOE high after FSMC_D[15:0] data is valid	15		
$t_{w\ (NWE)}$	FSMC_NWE low time	$4*t_{HCLK}$		
$t_{v\ (NWE\text{-}D)}$	FSMC_NWE low to FSMC_D[15:0] data valid	0		
$t_{h\ (NWE\text{-}D)}$	FSMC_NWE high to FSMC_D[15:0] data invalid	$2*t_{HCLK}$		
$t_{d\ (ALE\text{-}NWE)}$	FSMC_NWE low before FSMC_ALE valid	$2*t_{HCLK}$		
$t_{h\ (NWE\text{-}ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2*t_{HCLK}$		
$t_{d\ (ALE\text{-}NOE)}$	FSMC_NOE low before FSMC_ALE valid	$2*t_{HCLK}$		
$t_{h\ (NOE\text{-}ALE)}$	FSMC_NOE high to FSMC_ALE invalid	$4*t_{HCLK}$		

3.3.22 QSPI Characteristics

Table 3-39 QSPI characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	QSPI clock frequency			90	MHz
$t_{r(SCK)}/t_{f(SCK)}$	QSPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	f_{HCLK} = 24MHz, pre-division coefficient = 4	70	97	ns
$t_{SU(SIO*)}$	Data input setup time		15		ns
$t_{h(SIO*)}$	Data input holding time		4		ns
$t_{V(SIO*)}$	Data output setup time			5	ns
$t_{h(SIO*)}$	Data output holding time		0		ns

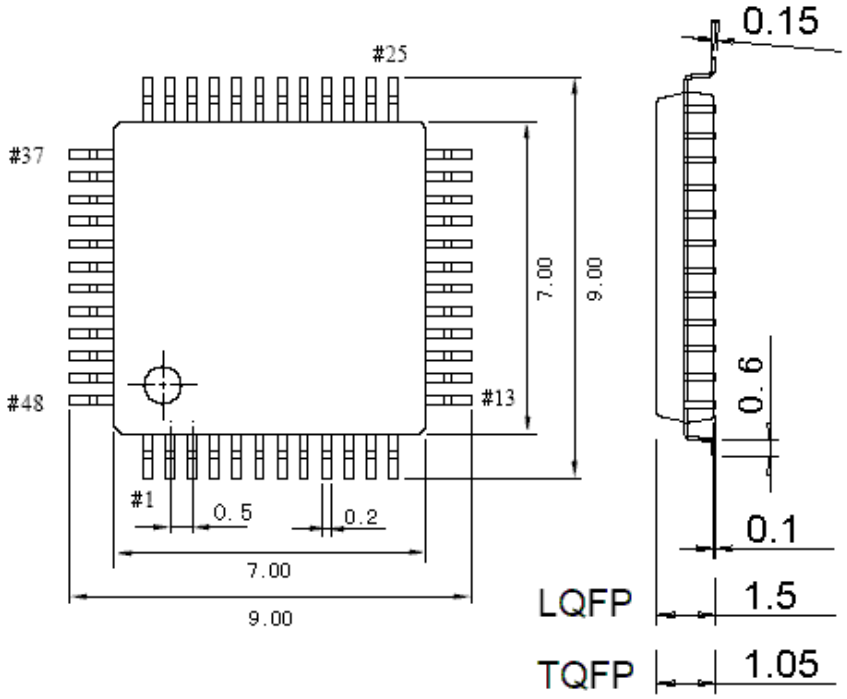
Chapter 4 Package and Ordering Information

Packages

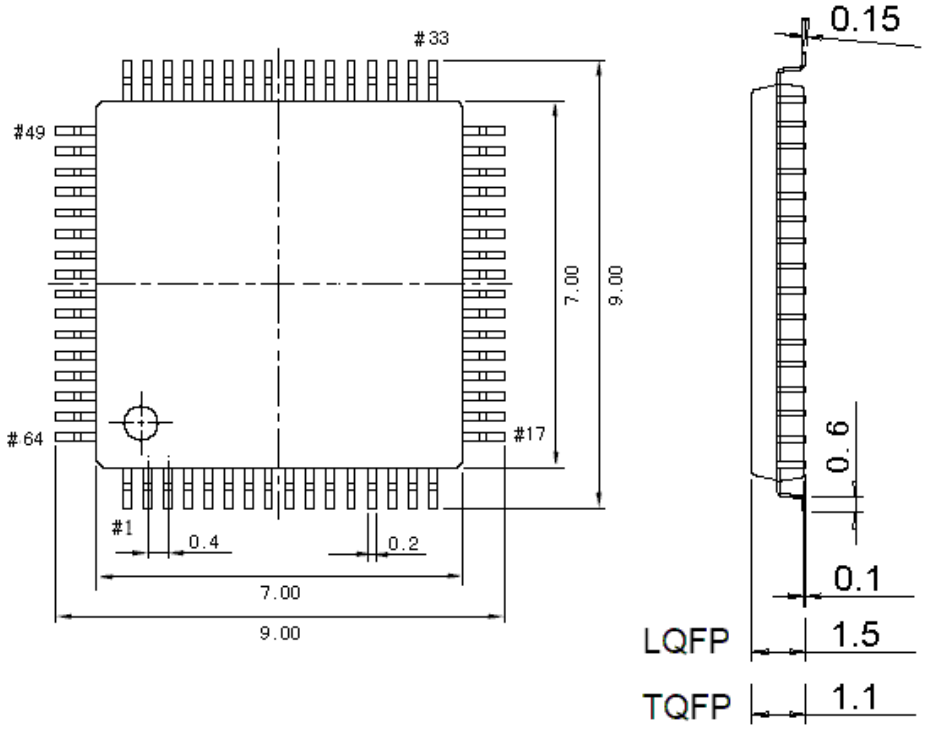
Package Form	Body size	Pin Pitch		Package Description	Order Model
LQFP48	7*7mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V205CCT6
LQFP64	7*7mm	0.4mm	15.7mil	Low Profile Quad Flat Pack	CH32V205RCT6
LQFP100	14*14mm	0.5mm	19.7mil	Quad Flat No-lead Package	CH32V205VCT6
LQFP48	7*7mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V203CCT6

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or ±10%.

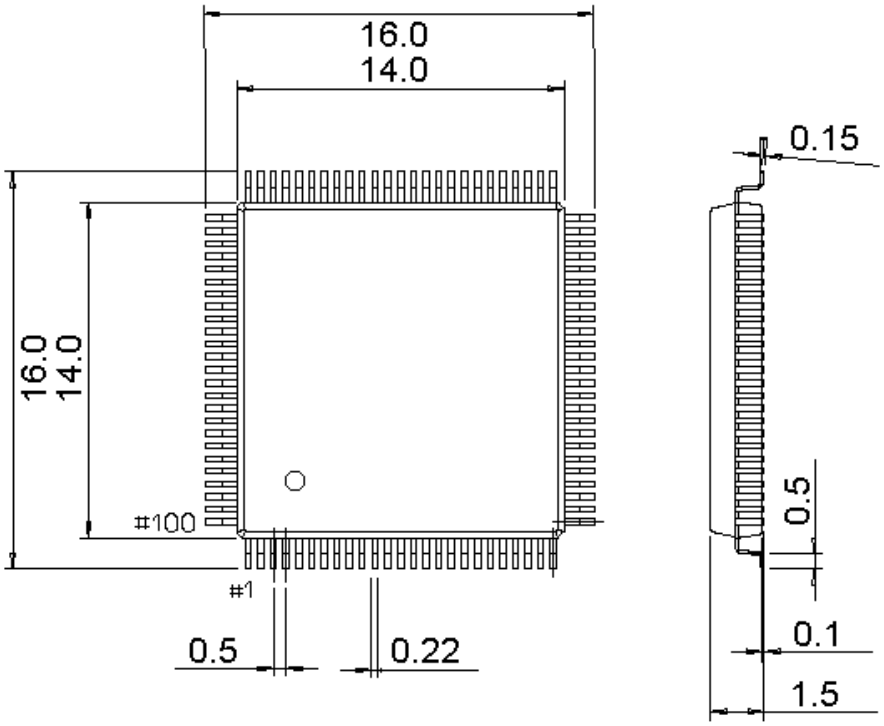
4.1 LQFP48 Package



4.2 LQFP64 Package



4.3 LQFP100 Package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Product Series

F = Arm core, general-purpose MCU
V = QingKe RISC-V core, general-purpose MCU
L = QingKe RISC-V core, low-power MCU
X = QingKe RISC-V core, dedicated or special peripheral MCU
M = QingKe RISC-V core, Built-in gate drive motor MCU
H = QingKe RISC-V core, high-performance MCU

Product type (*)+Product sub-series (**)

Product type	Product sub-series
0 = Value version, main frequency <=48M	02 = 16K Flash value general-purpose type 03 = 16K Flash basic general-purpose type, OPA 06 = 64K Flash multi-function general-purpose type, OPA, dual-purpose, TKey 07 = Basic motor application type, OPA+CMP
1 = Basic version, main frequency <=100M 2 = Enhanced version, main frequency <=200M 3 = Hardware floating point, medium and large capacity <512KB	03 = Connected, USB 05 = Connected, USB HS, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (Built-in PHY), SDIO
4 = Hardware floating point, large capacity >=512KB	17 = Interconnected, USB SS, SerDes, HSADC, UHSIF, SDIO, DVP, Ethernet (Built-in PHY)

Pin number

J = 8 pin D = 12 pin A = 16 pin F = 20 pin E = 24 pin
G = 28 pin K = 32 pin T = 36 pin C = 48 pin R = 64 pin
W = 68 pin M = 88 pin V = 100 pin Q = 128 pin Z = 144 pin

Flash memory capacity

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory 8 = 64K Flash memory
B = 128K Flash memory C = 256K Flash memory E = 512K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40℃~85℃ (Industrial-grade) 7 = -40℃~105℃(Automotive-grade 2 or extended industrial-grade)
3 = -40℃~125℃ (Automotive-grade 1) D = -40℃~150℃ (Automotive-grade 0)