



GD25R256D

DATASHEET



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1. FEATURES

- ◆ 256M-bit Serial Flash
 - 256 Bytes per programmable page
- ◆ Standard, Dual, Quad SPI
 - Standard SPI: SCLK, CS#, SI, SO
 - Dual SPI: SCLK, CS#, IO0, IO1
 - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
 - 3- or 4-Byte Addressing Mode
- ◆ High Speed Clock Frequency
 - 104MHz for Standard and Dual SPI fast read with 30PF load
 - Dual I/O Data transfer up to 208Mbits/s
 - Quad I/O Data transfer up to 416Mbits/s
- ◆ Software Write Protection
 - Write protect all/portion of memory via software
 - Top/Bottom Block protection
- ◆ Endurance and Data Retention
 - Minimum 100,000 Program/Erase Cycles
 - 20-year data retention typical
- ◆ Allows XiP (eXecute in Place) Operation
 - High speed Read reduce overall XiP instruction fetch time
 - Continuous Read with Wrap further reduce data latency to fill up SoC cache
- ◆ Fast Program/Erase Speed
 - Page Program time: 0.4ms typical
 - Sector Erase time: 70ms typical
 - Block Erase time: 0.16/0.22s typical
 - Chip Erase time: 70s typical
- ◆ Flexible Architecture
 - Uniform Sectors of 4K-Byte
 - Uniform Blocks of 32/64K-Byte
- ◆ Low Power Consumption
 - 2uA typical deep power down current
 - 13uA typical standby current
- ◆ Advanced Security Features
 - 3x2048-Byte Security Registers With OTP Locks
 - 128-bit Unique ID
 - Serial Flash Discoverable parameters (SFDP) register
 - Replay Protected Monotonic Counter (RPMC) function
- ◆ Single Power Supply Voltage
 - Full voltage range: 2.7 - 3.6V
- ◆ Package Information
 - SOP16 (300mil)
 - WSON8 (8*6mm)
 - TFBGA-24 (5*5 ball array)

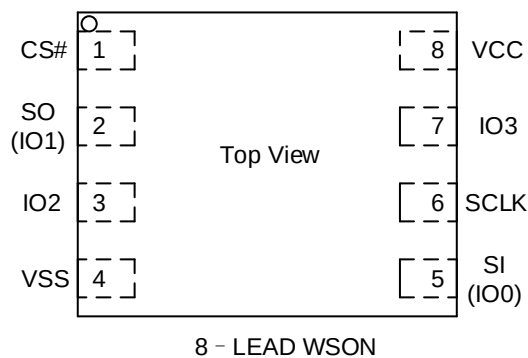
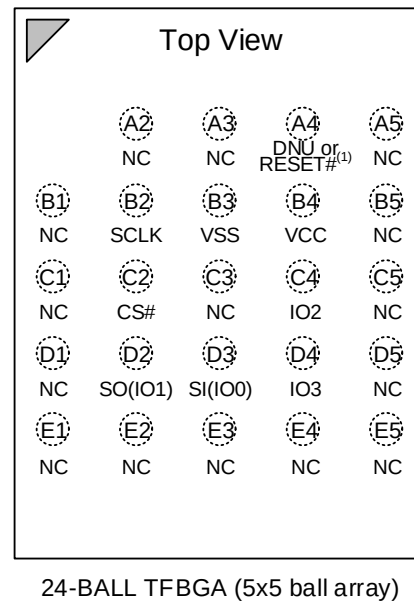
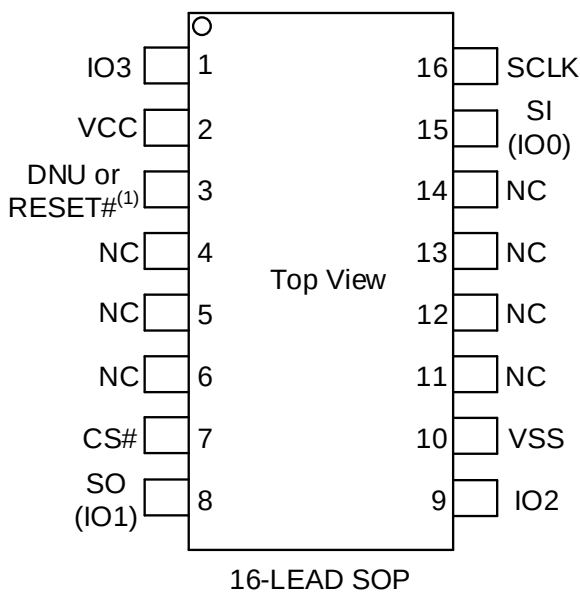


2. GENERAL DESCRIPTION

The GD25R256D (256M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, and I/O3. The Dual I/O data is transferred with speed of 208Mbits/s and the Quad I/O & Quad output data is transferred with speed of 416Mbits/s.

CONNECTION DIAGRAM

Figure 1 Connection Diagram



Note:

1. Dedicated RESET# pin (Pin 3 of 16-LEAD SOP package or Pin A4 of 24-BALL TFBGA package) is available through special order. Please refer to Chapter 9 for detailed ordering information.
2. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.



PIN DESCRIPTION

Table 1. Pin Description for SOP16 package

Pin No.	Pin Name	I/O	Description
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	DNU or RESET#	I	Do Not Use or RESET Input
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	IO2	I/O	Data Input Output 2
10	VSS		Ground
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input

Table 2 Pin Description for TFBGA24 package

Pin No.	Pin Name	I/O	Description
A4	DNU or RESET#	I	Do Not Use or RESET Input
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C4	IO2	I/O	Data Input Output 2
D2	SO (IO1)	I/O	Data Output (Data Input Output 1)
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)
D4	IO3	I/O	Data Input Output 3

Table 3 Pin Description for WSON8 package

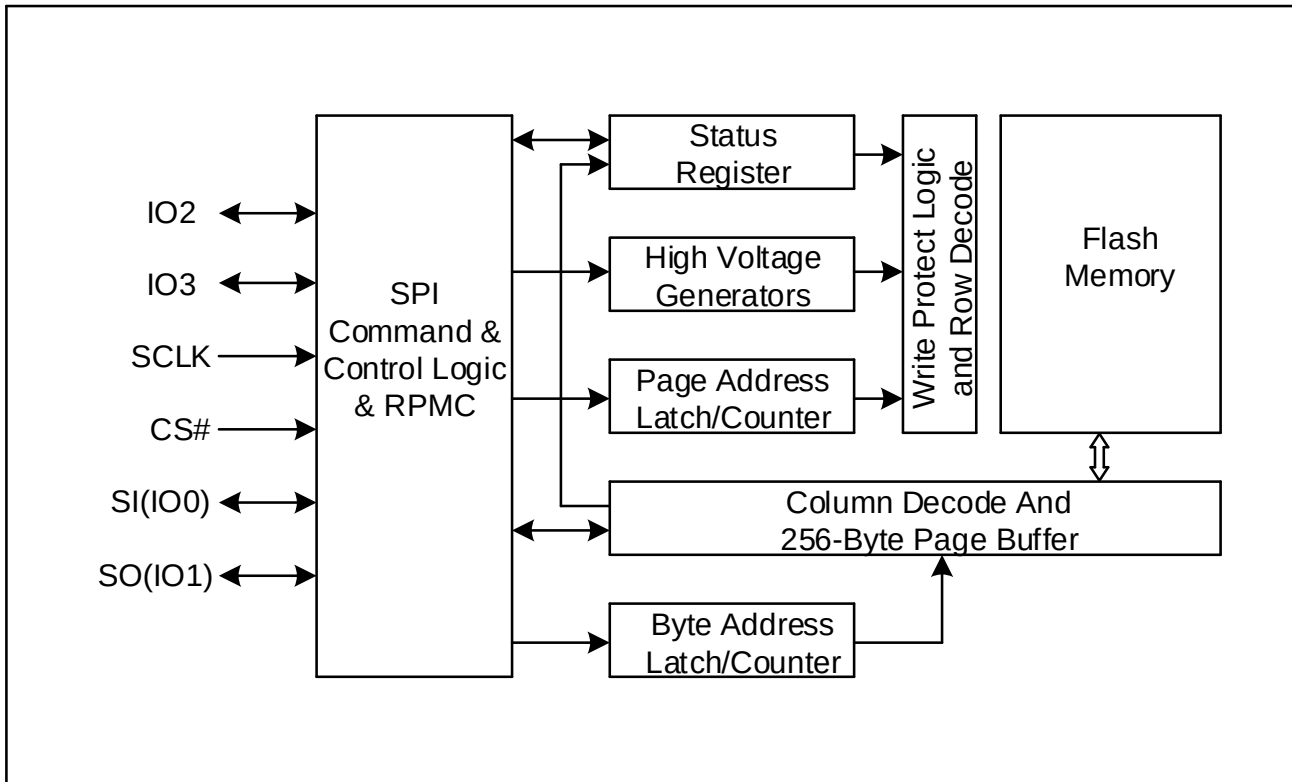
Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	IO2	I/O	Data Input Output 2
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3
8	VCC		Power Supply

Note: CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.



BLOCK DIAGRAM

Figure 2 Block Diagram





3. MEMORY ORGANIZATION

GD25R256D

Table 4 GD25R256D Memory Organization

Each device has	Each block has	Each sector has	Each page has	
32M	64/32K	4K	256	Bytes
128K	256/128	16	-	pages
8192	16/8	-	-	sectors
512/1024	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25R256D

Table 5 GD25R256D 64K Bytes Block Sector Architecture

Block	Sector	Address Range	
511	8191	01FF F000H	01FF FFFFH
			
	8176	01FF 0000H	01FF 0FFFH
510	8175	01FE F000H	01FE FFFFH
			
	8160	01FE 0000H	01FE 0FFFH
509	8159	01FD F000H	01FD FFFFH
			
	8144	01FD 0000H	01FD 0FFFH
.....			
			
			
.....			
			
			
2	47	0002 F000H	0002 FFFFH
			
	32	0002 0000H	0002 0FFFH
1	31	0001 F000H	0001 FFFFH
			
	16	0001 0000H	0001 0FFFH
0	15	0000 F000H	0000 FFFFH
			
	0	0000 0000H	0000 0FFFH



4. DEVICE OPERATION

SPI Mode

Standard SPI

The GD25R256D features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25R256D supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-Byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-Byte address” commands (3BH 3CH BBH and BCH). These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25R256D supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad Output Fast Read with 4-Byte address”, “Quad I/O Fast Read”, “Quad I/O Fast Read with 4-Byte address” (6BH, 6CH, EBH and ECH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For GD25R256D, QE bit is set to 1 as default and cannot be changed.



5. DATA PROTECTION

The GD25R256D provides the following data protection methods:

- ◆ Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
 - Power-Up/Software reset (66H+99H)
 - Write Disable (WRDI)
 - Write Status Register (WRSR)
 - Page Program (PP)
 - Quad Page Program (QPP)
 - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- ◆ Software Protection Mode:
 - The Block Protect (BP3, BP2, BP1, and BP0) bits and Top Bottom (TB) bit define the section of the memory array that can be read but cannot be change.
- ◆ Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and software reset (66H+99H).

Table 6. GD25R256D Protected area size

Status Register Content					Memory Content			
TB	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h-01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h-01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h-01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h-01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 to 511	01F00000h-01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h-01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h-01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h-01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h-01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h-0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h-0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h-0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h-0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h-000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h-001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 to 63	00000000h-003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h-007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h-00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	ALL	00000000h-01FFFFFFh	32MB	ALL
X	1	X	1	X	ALL	00000000h-01FFFFFFh	32MB	ALL



6. STATUS AND EXTENDED ADDRESS REGISTERS

6.1. Status Registers

Table 7 Status Register-1

No.	Bit Name	Description	Note
S0	WIP	Erase/Write In Progress	Volatile, read only
S1	WEL	Write Enable Latch	Volatile, read only
S2	BP0	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S6	TB	Top/Bottom Protect Bit	Non-volatile writable
S7	SRP0	Status Register Protection Bit	Non-volatile writable

Table 8 Status Register-2

No.	Bit Name	Description	Note
S8	ADS	Current Address Mode	Volatile, read only
S9	QE	Quad Enable	QE=1 permanently
S10	SUS2	Program Suspend	Volatile, read only
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S14	SRP1	Status Register Protection Bit	Non-volatile writable
S15	SUS1	Erase Suspend	Volatile, read only

Table 9 Status Register-3

No.	Bit Name	Description	Note
S16	Reserved	Reserved	Reserved
S17	Reserved	Reserved	Reserved
S18	PE	Program Error bit	Volatile, read only
S19	EE	Erase Error bit	Volatile, read only
S20	ADP	Power Up Address Mode	Non-volatile writable
S21	DRV0	Output Driver Strength	Non-volatile writable
S22	DRV1	Output Driver Strength	Non-volatile writable
S23	Reserved	Reserved	Reserved

The status and control bits of the Status Register are as follows (The Status Register is not used for RPMC):

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.



WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

TB bit

The Top Bottom (TB) bit is non-volatile (OTP). The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, and BP0), starting from Top or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set to “1”, the protect area will change to Bottom area of the memory device. This bit is written with the Write Status Register (WRSR) command.

BP3, BP2, BP1, BP0 bits

The Block Protection (BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, and BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Chip Erase (CE) command is executed, only if the Block Protect (BP3, BP2, BP1, and BP0) bits are 0.

SRP1, SRP0 bit

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of the write protection: software protected, power supply lock-down or one time programmable.

Table 10 Status Register Protect (SRP) bit

SRP1	SRP0	Status Register	Description
0	0	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Power Supply Lock-Down ^{(1) (2)}	Status Register is protected and cannot be written to again until the nest Power-Down, Power-Up cycle
1	1	One Time Program ⁽²⁾	Status Register is permanently protected and cannot to written to.

NOTE:

1. When SRP1, SRP0 = (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact GigaDevice for details.

QE bit

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 1 and it cannot be changed, so that the IO2 and IO3 pins are enabled all the time.

LB3, LB2, LB1 bits.

The LB3, LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S11, S12, S13) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1 are 0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

SUS1, SUS2 bits

The SUS1 and SUS2 bits are read only bit in the status register (S15 and S10) that are set to 1 after executing an



Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

PE bit

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

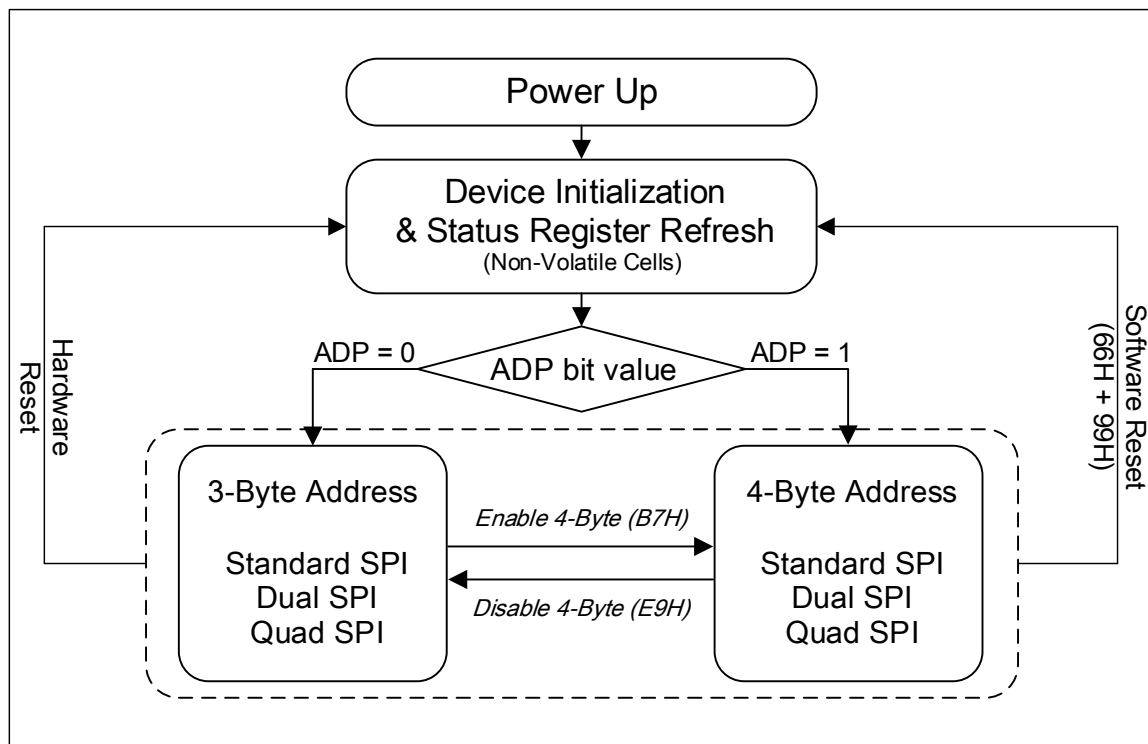
EE bit

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

ADP bit

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0 (factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.



ADS bit

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

DRV1, DRV0 bits

The DRV1&DRV0 bits are used to determine the output driver strength for the Read operations.



Table 11 Driver Strength for Read Operations

DRV1,DRV0	Driver Strength
00	100%
01	75% (Default)
10	Reserved
11	Reserved

Reserved bit

It is recommended to set the value of the reserved bit as "0".



6.2. Extended Address Register

Table 12 Extended Address Register

No.	Name	Description	Note
EA0	A24	Address bit	Volatile writable
EA1	Reserved	Reserved	Reserved
EA2	Reserved	Reserved	Reserved
EA3	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA5	Reserved	Reserved	Reserved
EA6	Reserved	Reserved	Reserved
EA7	Reserved	Reserved	Reserved

The extended address register is only used when the address mode is 3-Byte mode, as to set the higher address. A24=1 indicates the upper 128Mb memory address, A24=0 indicates the lower 128Mb. EA1~EA7 are reserved.

A24 bit

The Extended Address Bit A24 is used only when the device is operating in the 3-Byte Address Mode (ADS=0), which is volatile writable by C5H command. The lower 128Mb memory array (00000000h – 00FFFFFFh) is selected when A24=0, and all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (01000000h – 01FFFFFFh) will be selected.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit A24 setting will be ignored. However, any instruction with 4-Byte address input will replace the Extended Address Bit A24 with new settings.

Reserved bit

It is recommended to set the value of the reserved bit as “0”.



7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-Byte command code must be shifted in to the device, with most significant bit first on SI, and each bit being latched on the rising edges of SCLK.

Every command sequence starts with a one-Byte command code. Depending on the command, this might be followed by address Bytes, or by data Bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a Byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input Byte is not a full Byte, nothing will happen and WEL will not be reset.

When the device is in 3-Byte address mode (ADS=0), please refer to command set in table13 & table14. When the device is in 4-Byte address mode (ADS=1), please refer to command set in table13 & table15.

Extended Address Register setting is effective to achieve A31-A24, accompanying A23-A0 within the instruction, when commands listed in table14 are executed.

Extended Address Register setting is ignored when A31-A24 are given in the instruction listed in table 15 and some specific instruction from table13 (13H, 0CH, 3CH, 6CH, BCH, ECH).

Table 13. Commands (Standard/Dual/Quad SPI, 3-Byte & 4-Byte address mode)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	3 & 4	06H						
Write Disable	3 & 4	04H						
Volatile SR Write Enable	3 & 4	50H						
Read Status Register-1	3 & 4	05H	(S7-S0)					(cont.)
Read Status Register-2	3 & 4	35H	(S15-S8)					(cont.)
Read Status Register-3	3 & 4	15H	(S23-S16)					
Write Status Register-1	3 & 4	01H	S7-S0					
Write Status Register-1&2	3 & 4	01H	S7-S0	S15-S8				
Write Status Register-2	3 & 4	31H	S15-S8					
Write Status Register-3	3 & 4	11H	S23-S16					
Read Extended Addr. Register	3 & 4	C8H	(EA7-EA0)					
Write Extended Addr. Register	3 & 4	C5H	EA7-EA0					



Uniform Sector GigaDevice Dual and Quad Serial Flash

GD25R256D

Chip Erase	3 & 4	C7/60H						
Enable Reset	3 & 4	66H						
Reset	3 & 4	99H						
Program/Erase Suspend	3 & 4	75H						
Program/Erase Resume	3 & 4	7AH						
Set Burst with Wrap ⁽⁵⁾	3 & 4	77H	dummy W7-W0					
Release From Deep Power-Down	3 & 4	ABH						
Read Device ID	3 & 4	ABH	dummy	dummy	dummy	(DID7-DID0)		(cont.)
Deep Power-Down	3 & 4	B9H						
Manufacturer/Device ID	3 & 4	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(cont.)
Manufacturer/Device ID by Dual I/O	3 & 4	92H	A23-A8	A7-A0, M7-M0	(MID7-MID0) (DID7-DID0)			
Manufacturer/Device ID by Quad I/O	3 & 4	94H	A23-A0, M7-M0	dummy ⁽⁵⁾ (MID7-MID0) (DID7-DID0)				
Read Identification	3 & 4	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(cont.)
Enter 4-Byte Address Mode	3 & 4	B7H						
Exit 4-Byte Address Mode	3 & 4	E9H						
Read Data with 4-Byte Address	3 & 4	13H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	3 & 4	0CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address ⁽¹⁾	3 & 4	3CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Quad Output with 4-Byte Address ⁽³⁾	3 & 4	6CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual I/O with 4-Byte Address ⁽²⁾	3 & 4	BCH	A31-A24 A23-A 16	A15-A8 A7-A0	M7-M0 (D7-D0)			
Fast Read Quad I/O with 4-Byte Address ⁽⁴⁾	3 & 4	ECH	A31-A24 A23-A 16 A15-A8 A7-A0	M7-M0 dummy dummy D7-D0				
Page Program with 4-Byte Address	3 & 4	12H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte
Quad Page	3 & 4	34H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	



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Program with 4-Byte Address								
Sector Erase with 4-Byte Address	3 & 4	21H	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase(32K) with 4-Byte Address	3 & 4	5CH	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase(64K) with 4-Byte Address	3 & 4	DCH	A31-A24	A23-A16	A15-A8	A7-A0		
Clear SR Flags	3 & 4	30H						
Read Serial Flash Discoverable Parameter	3 & 4	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)

Table 14 Commands (Standard/Dual/Quad SPI, 3-Byte address)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	3	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)	(cont.)
Fast Read	3	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Dual Output Fast Read ⁽¹⁾	3	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) ⁽¹⁾	(cont.)
Dual I/O Fast Read ⁽²⁾	3	BBH	A23-A8 ⁽²⁾	A7-A0 M7-M0 ⁽²⁾	(D7-D0) ⁽¹⁾			(cont.)
Quad Output Fast Read ⁽³⁾	3	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) ⁽³⁾	(cont.)
Quad I/O Fast Read ⁽⁴⁾	3	EBH	A23-A0 M7-M0 ⁽⁴⁾	dummy	(D7-D0) ⁽³⁾			(cont.)
Page Program	3	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte	
Quad Page Program	3	32H	A23-A16	A15-A8	A7-A0	D7-D0		
Sector Erase	3	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	3	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	3	D8H	A23-A16	A15-A8	A7-A0			
Read Unique ID	3	4BH	dummy	dummy	dummy	dummy	(UID7-UID0)	
Erase Security Registers ⁽⁶⁾	3	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers ⁽⁶⁾	3	42H	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	
Read Security Registers ⁽⁶⁾	3	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	



Table 15. Commands (Standard/Dual/Quad SPI, 4-Byte address)

Command Name	Add Mode	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Bytes-7	n-Bytes
Read Data	4	03H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)		(cont.)
Fast Read	4	0BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Dual Output Fast Read ⁽¹⁾	4	3BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) ⁽¹⁾	(cont.)
Dual I/O Fast Read ⁽²⁾	4	BBH	A31-A24 A23-A16	A15-A8 A7-A0	M7-M0 ⁽²⁾ dummy	(D7-D0) ⁽¹⁾			
Quad Output Fast Read ⁽³⁾	4	6BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) ⁽¹⁾	(cont.)
Quad I/O Fast Read ⁽⁴⁾	4	EBH	A31-A24 A23-A16 A15-A8 A7-A0	M7-M0 ⁽⁴⁾ dummy dummy (D7-D0) ⁽³⁾					(cont.)
Page Program	4	02H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	(cont.)
Quad Page Program	4	32H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0		(cont.)
Sector Erase	4	20H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(32K)	4	52H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(64K)	4	D8H	A31-A24	A23-A16	A15-A8	A7-A0			
Read Unique ID	4	4BH	dummy	dummy	dummy	dummy	dummy	(UID7-UID0)	
Erase Security Registers ⁽⁶⁾	4	44H	A31-A24	A23-A16	A15-A8	A7-A0			
Program Security Registers ⁽⁶⁾	4	42H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	(cont.)
Read Security Registers ⁽⁶⁾	4	48H	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)

NOTE:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0,)

IO1 = (D5, D1,)

IO2 = (D6, D2,)

IO3 = (D7, D3,.....)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Address, Continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID



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IO0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0, ...)

IO1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1, ...)

IO2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2, ...)

IO3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3, ...)

6. Security Registers Address

Security Register1: A23-A16=00H, A15-A12=1H, A11=0b, A10-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A12=2H, A11=0b, A10-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11=0b, A10-A0= Byte Address.

Table of ID Definitions:

GD25R256D

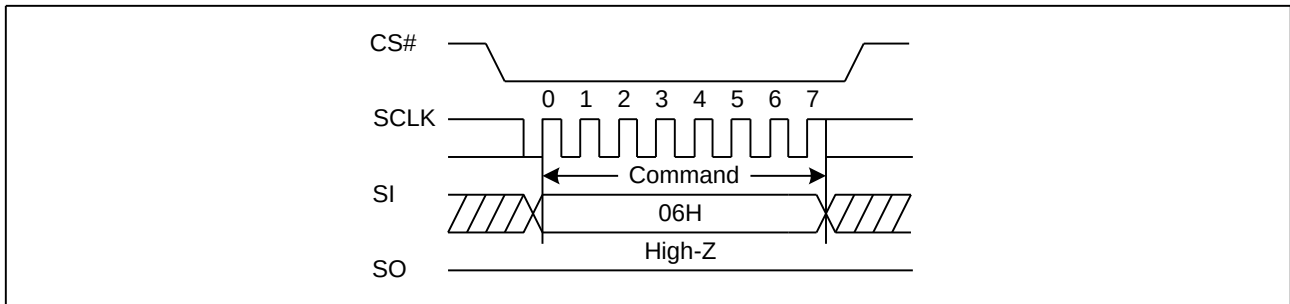
Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	40	19
90H	C8		18
ABH			18



7.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR). The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 3 Write Enable Sequence Diagram



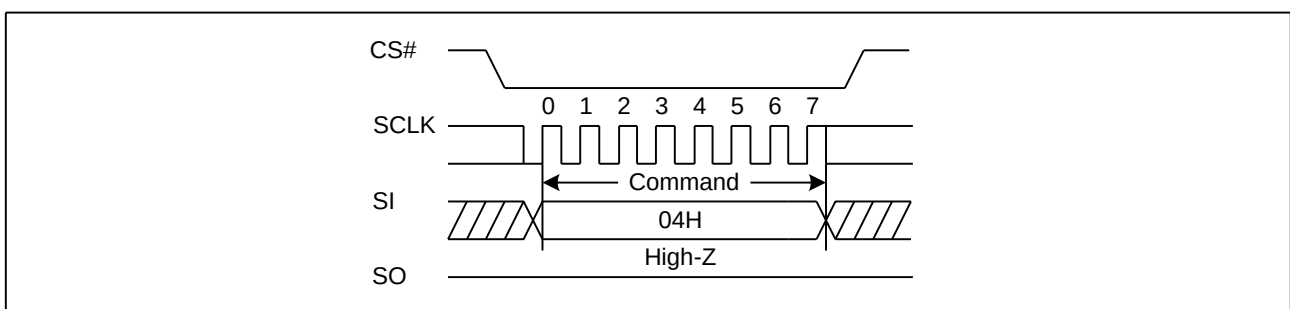
7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to a 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high.

Figure 4 Write Disable Sequence Diagram



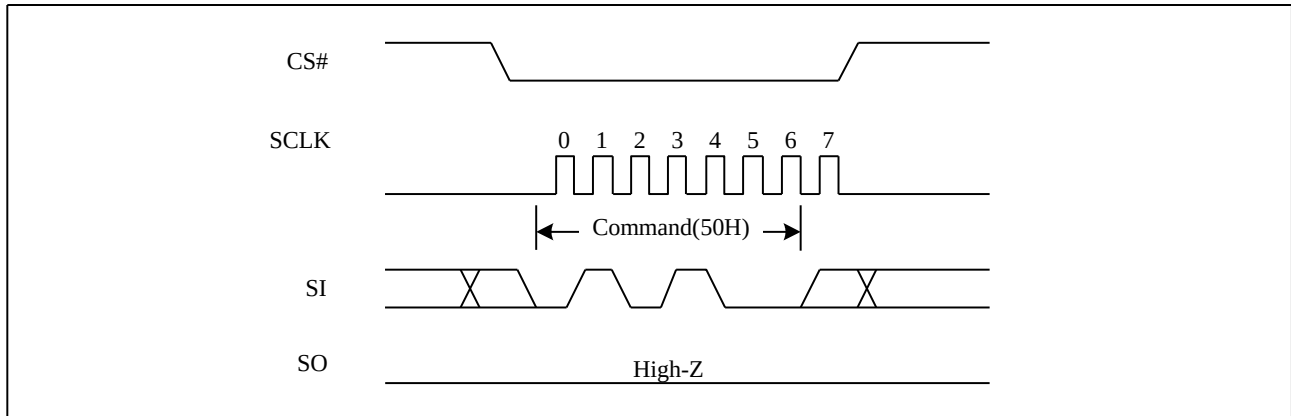
7.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status



Register bit values.

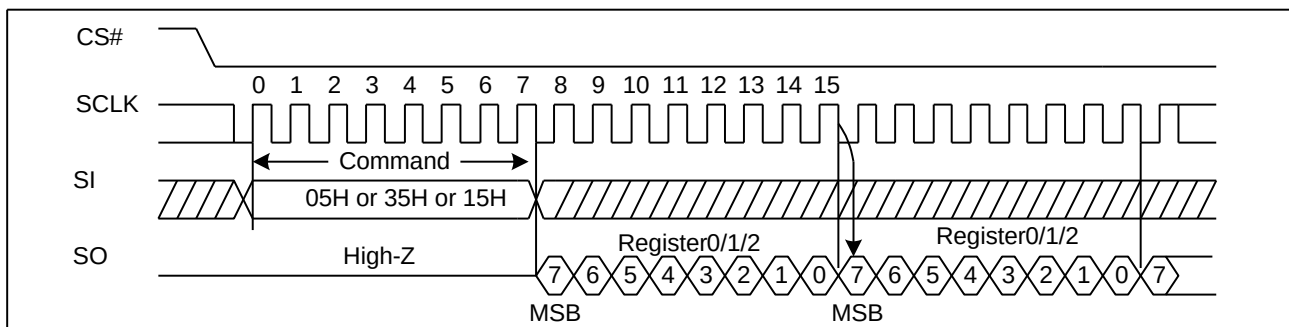
Figure 5. Write Enable for Volatile Status Register Sequence Diagram



7.4. Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H” / “35H” / “15H”, the SO will output Status Register bits S7~S0 / S15-S8 / S23-S16.

Figure 6 Read Status Register Sequence Diagram



7.5. Write Status Register (WRSR) (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S19, S18, S15, S10, S8, S1 and S0 of the Status Register. CS# must be driven high after the eighth of the data Byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_w) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

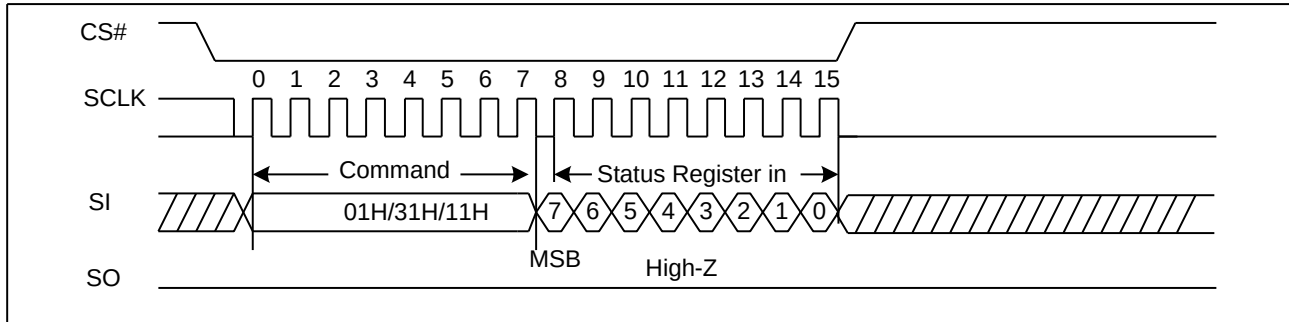
The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (TB, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only.

The Write Status Register-1 (01h) command can also write the Status Register-1&2. To complete the Write Status



Register-1&2 command, the CS# pin must be driven high after the sixteenth bit of data is clocked in. If CS# is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, and the Status Register-2 will not be affected.

Figure 7 Write Status Register Sequence Diagram

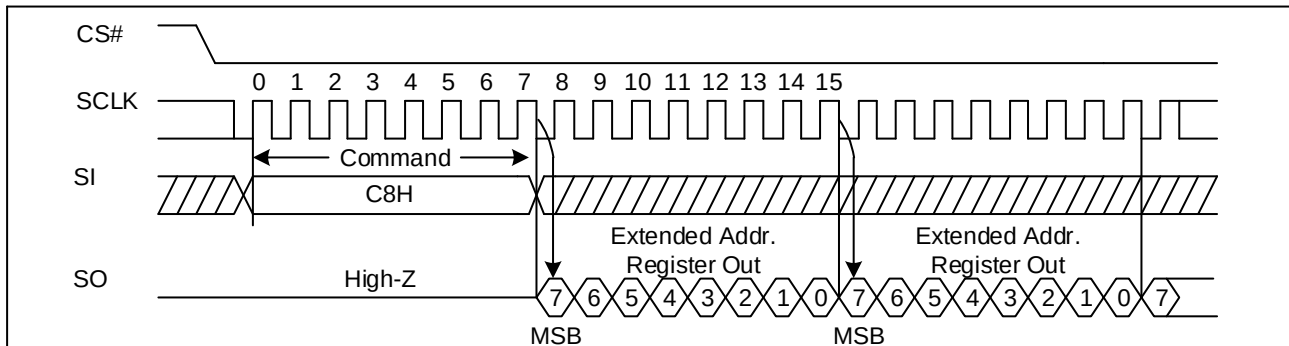


7.6. Read Extended Register (C8H)

Extended Register contains Address Bit A24. The Read Extended Register instruction is entered by driving CS# low and shifting the instruction code "C8H" into the SI pin on the rising edge of SCLK. The Extended Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 8.

When the device is in the 4-Byte Address Mode, the value of A24 Bit is ignored.

Figure 8 Read Extended Register Sequence Diagram

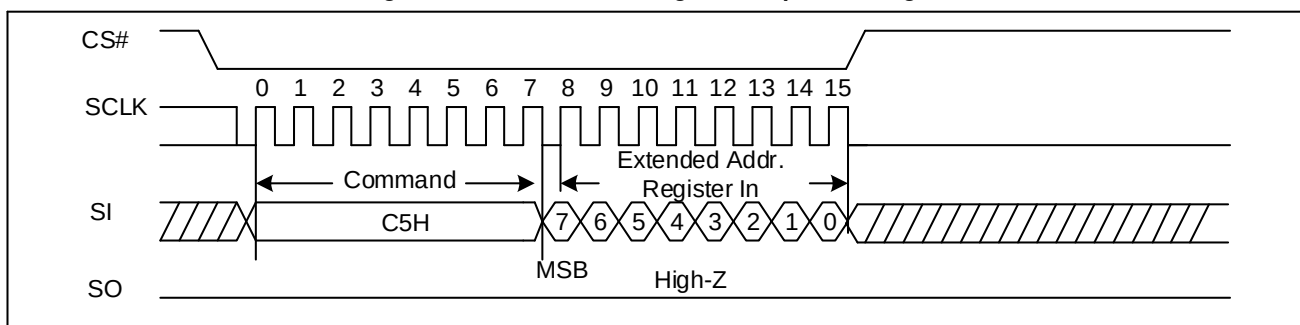


7.7. Write Extended Register (C5H)

The Write Extended Register command could be executed no matter the Write Enable Latch (WEL) bit is 0 or 1. The Write Extended Register instruction is entered by driving CS# low, sending the instruction code "C5H", and then writing the Extended Register data Byte as illustrated in Figure 9.

Upon power up or the execution of a Software/Hardware Reset, the Extended Register bit values will be cleared to 0.

Figure 9 Write Extended Register Sequence Diagram





7.8. Read Data Bytes (READ 03H or 4READ 13H)

The Read Data Bytes (READ) command is followed by a 3-Byte address (A23-A0), and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency f_R , on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 10 Read Data Bytes Sequence Diagram (ADS=0)

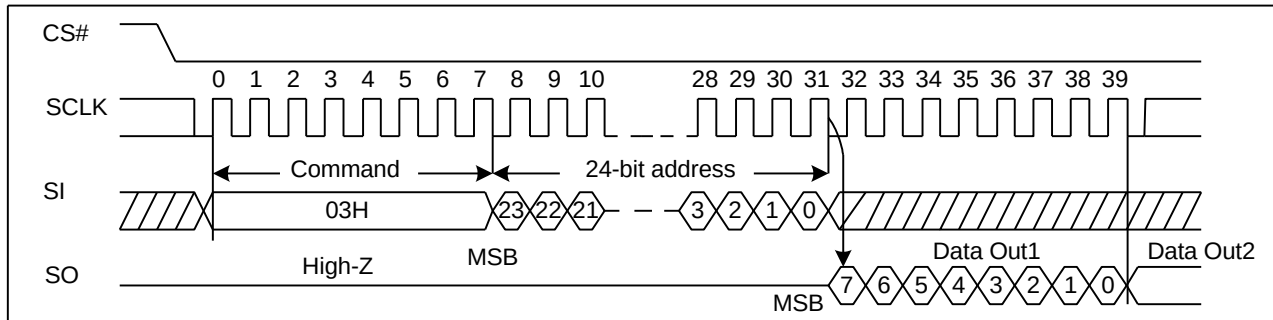


Figure 11 Read Data Bytes Sequence Diagram (ADS=1)

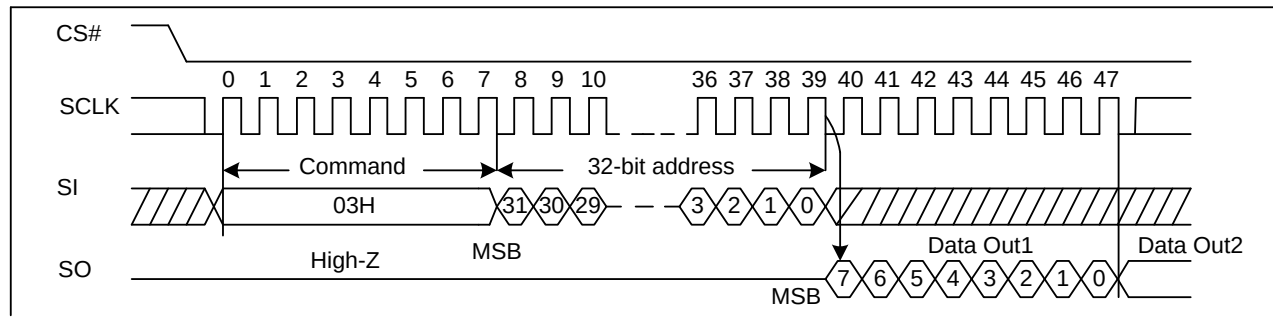
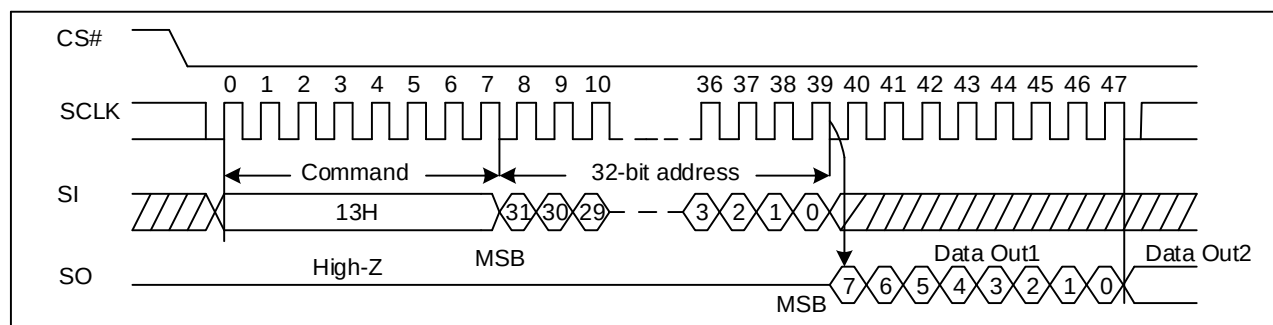


Figure 12 Read Data with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.9. Read Data Bytes at Higher Speed (Fast Read 0BH or 4Fast Read 0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency f_c , on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 13 Read Data Bytes at Higher Speed Sequence Diagram (ADS=0)

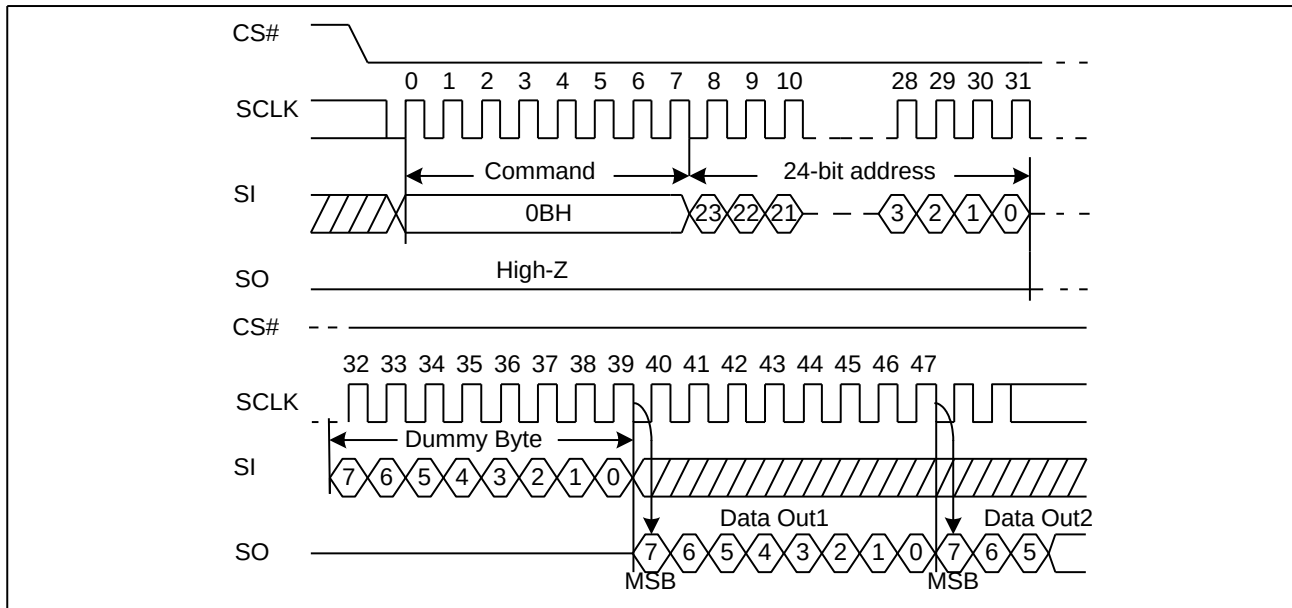


Figure 14 Read Data Bytes at Higher Speed Sequence Diagram (ADS=1)

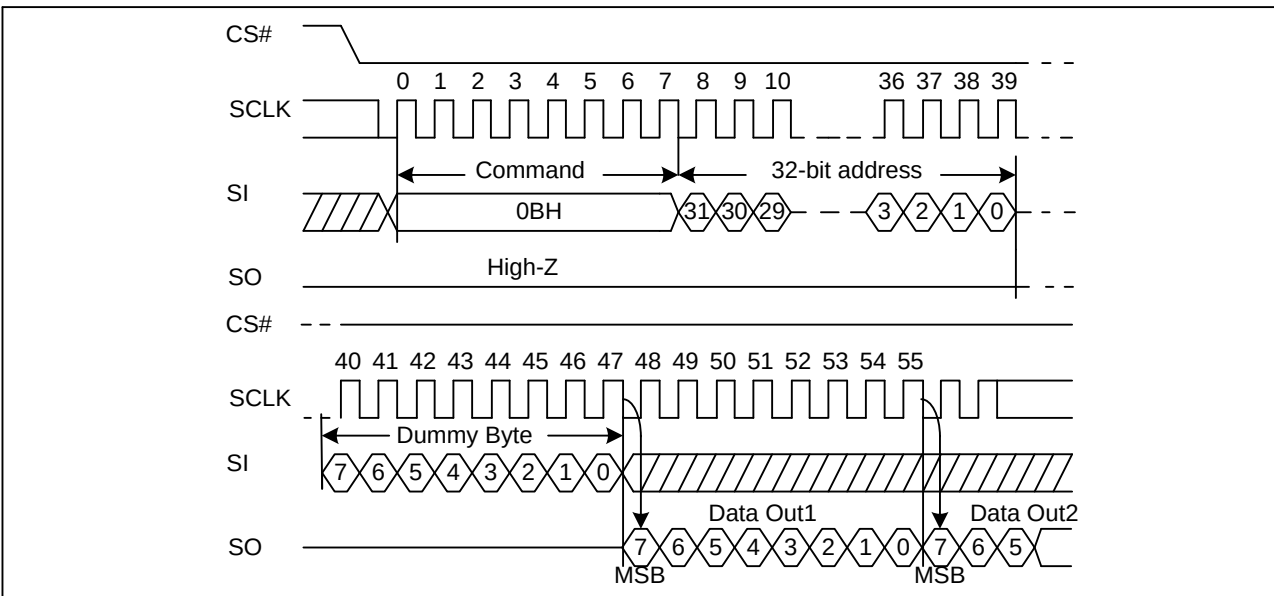
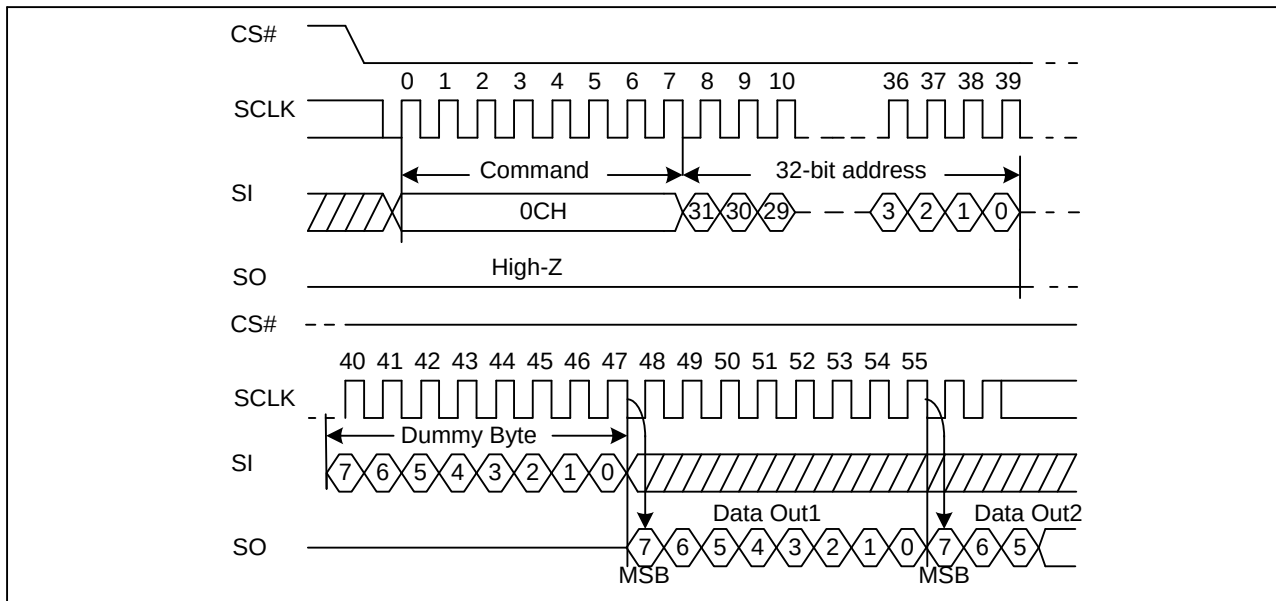




Figure 15 Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.10. Dual Output Fast Read (DOFR 3BH or 4DOFR 3CH)

The Dual Output Fast Read command is followed by 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure 16. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 16 Dual Output Fast Read Sequence Diagram (ADS=0)

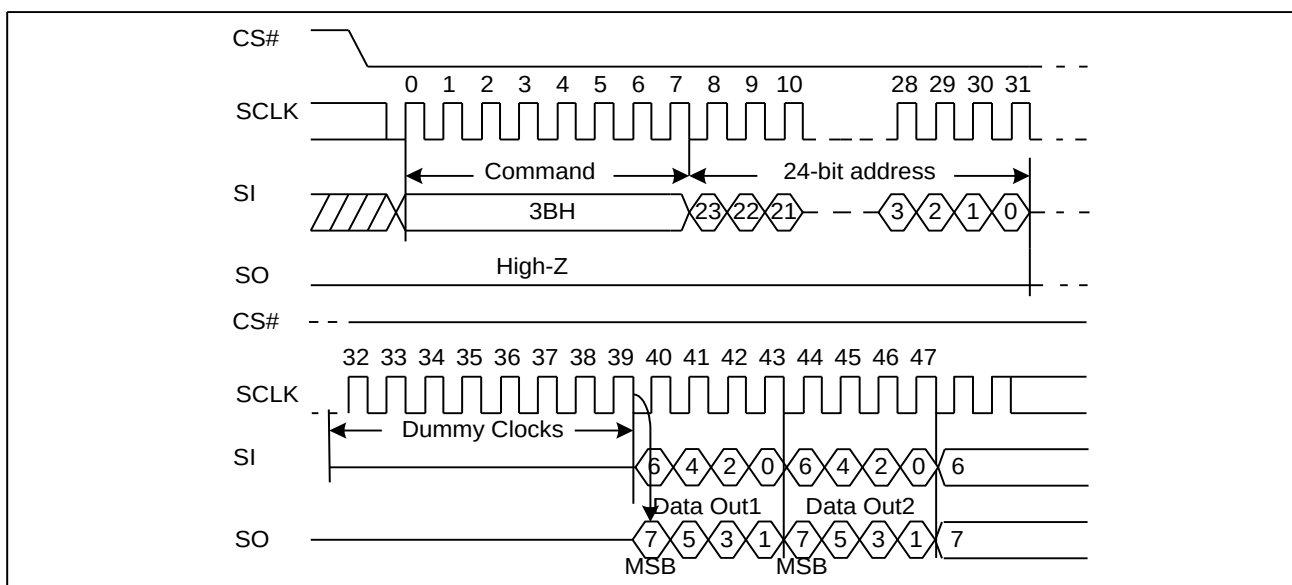




Figure 17 Dual Output Fast Read Sequence Diagram (ADS=1)

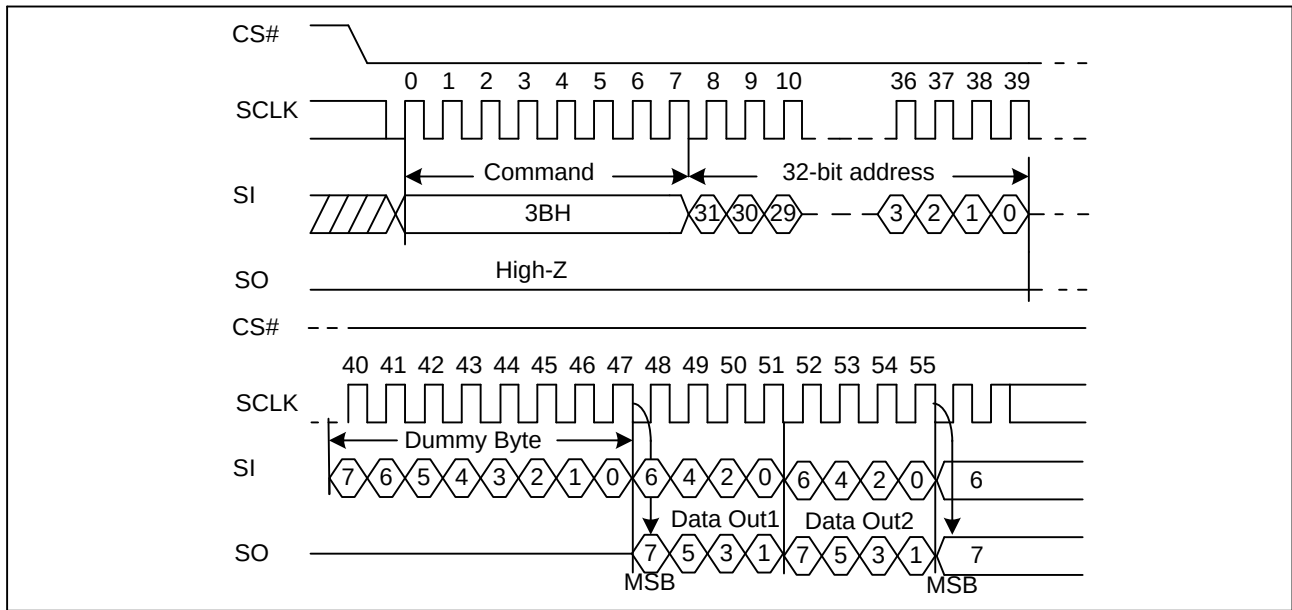
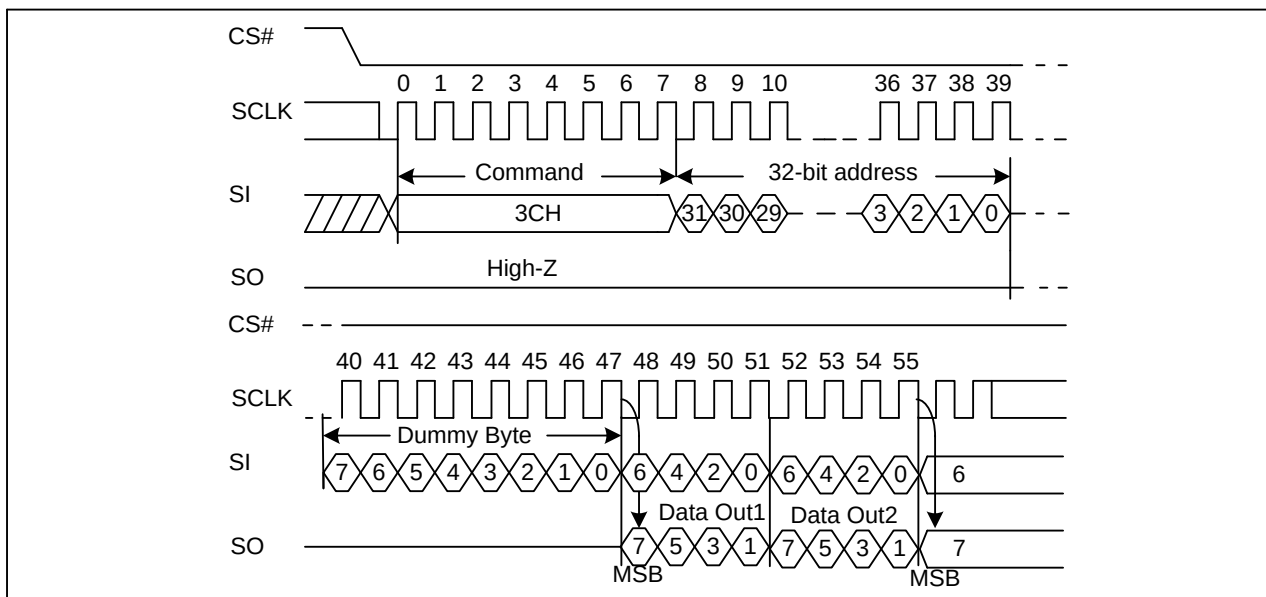


Figure 18 Dual Output Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.11. Quad Output Fast Read (QOFR 6BH or 4QOFR 6CH)

The Quad Output Fast Read command is followed by 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure19. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 19 Quad Output Fast Read Sequence Diagram (ADS=0)

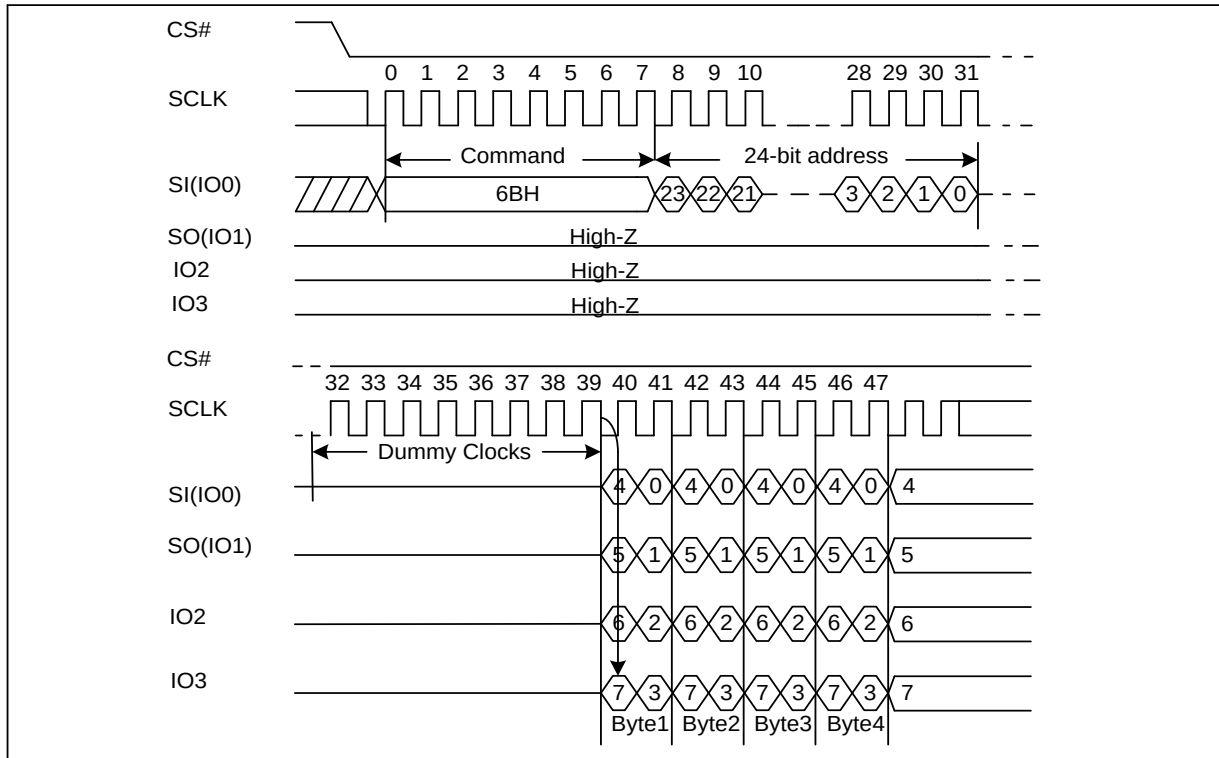




Figure 20 Quad Output Fast Read Sequence Diagram (ADS=1)

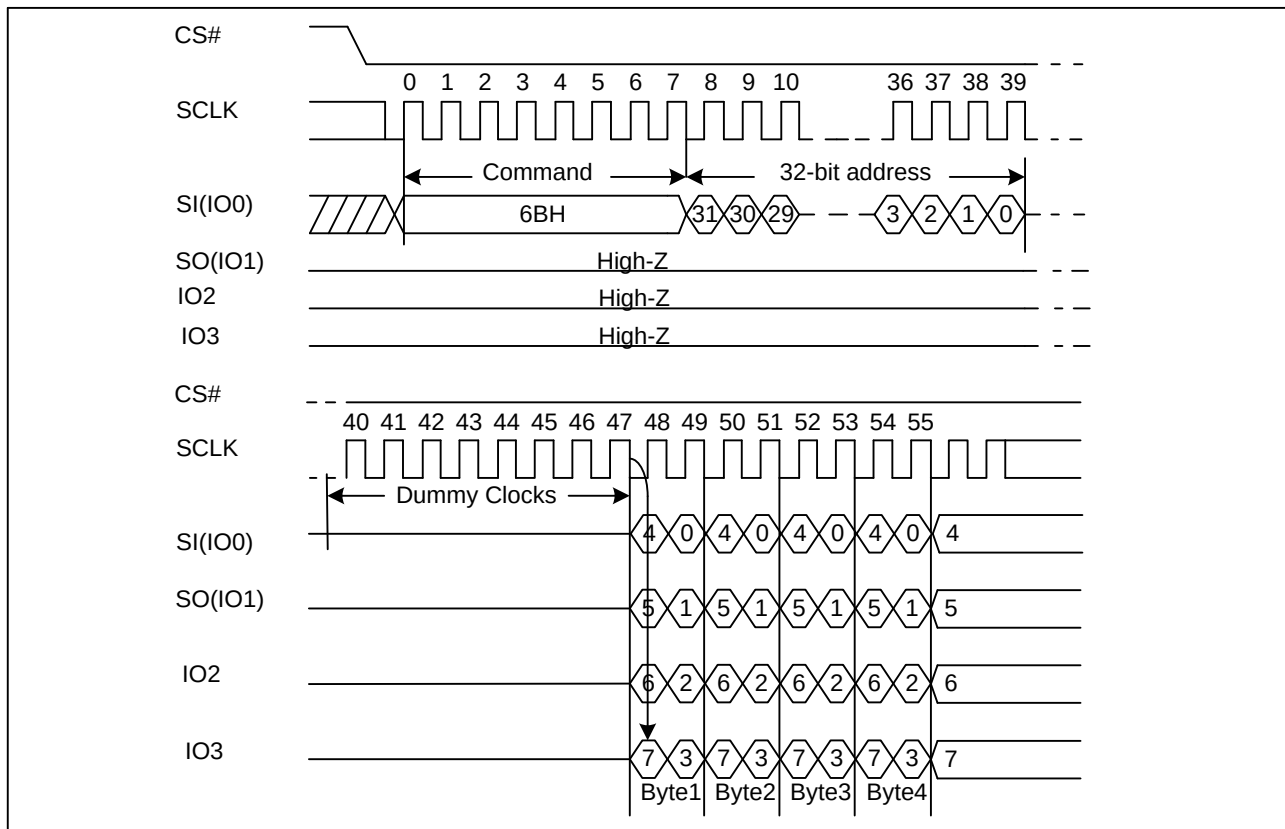
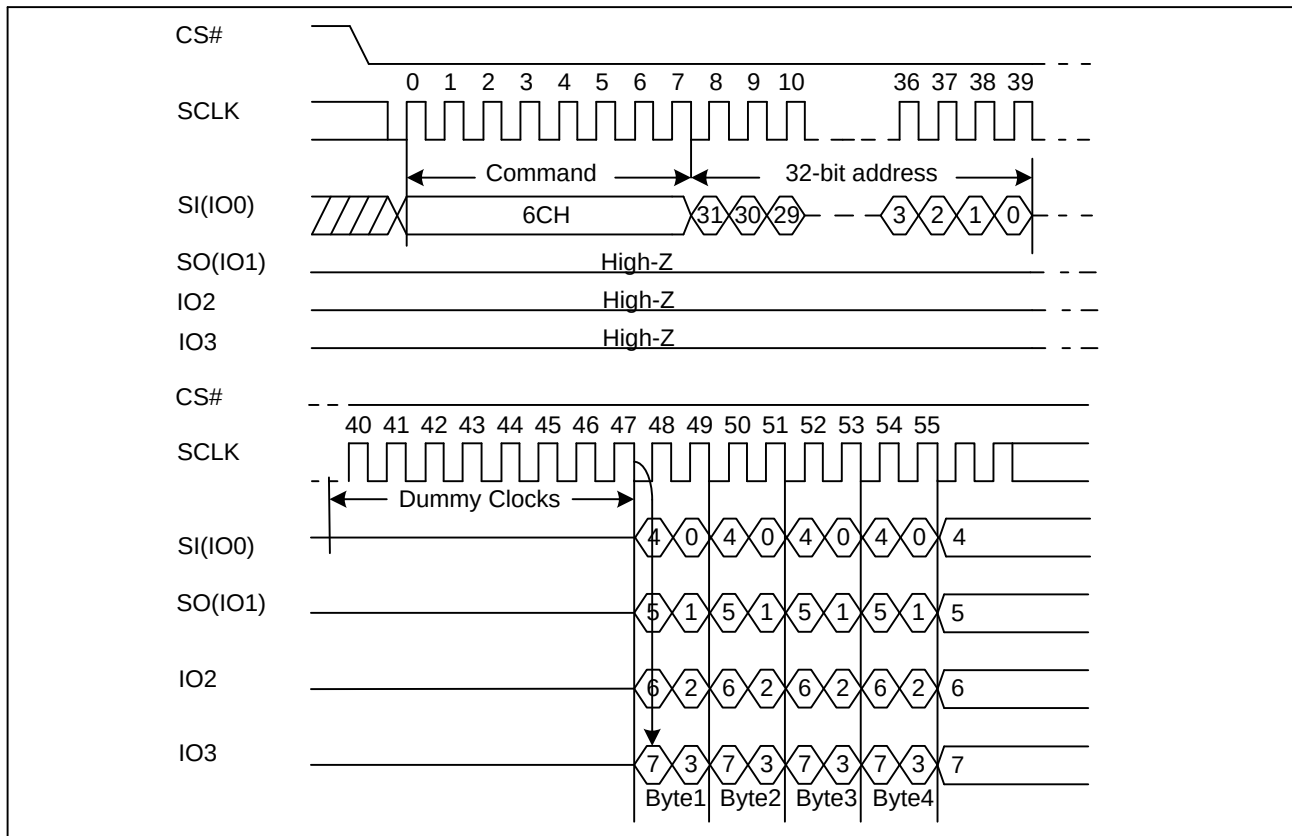




Figure 21 Fast Read Quad Output with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



7.12. Dual I/O Fast Read (DIOFR BBH or 4DIOFR BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-Byte address (A23-0) and a “Continuous Read Mode” Byte 2-bit per clock by SI and SO, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure22. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-4) after the input 3-Byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure23. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.



Figure 22 Dual I/O Fast Read Sequence Diagram (M5-4# (1, 0), ADS=0)

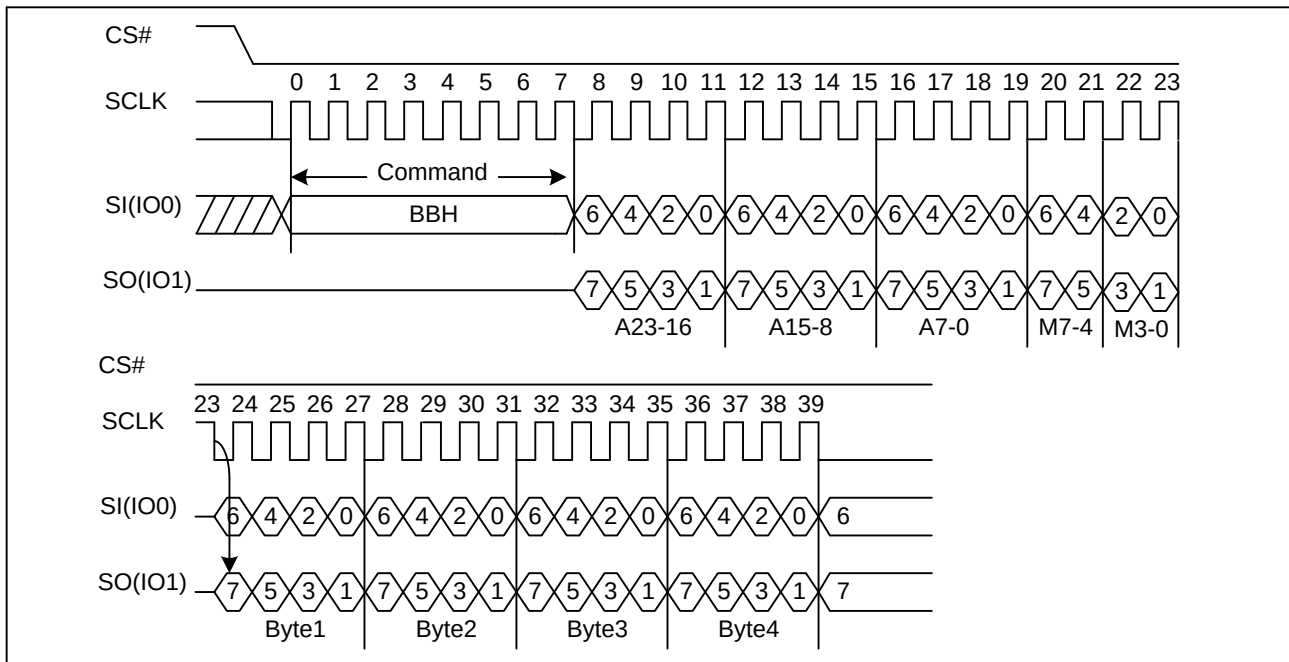


Figure 23 Dual I/O Fast Read Sequence Diagram (M5-4# (1, 0), ADS=0)

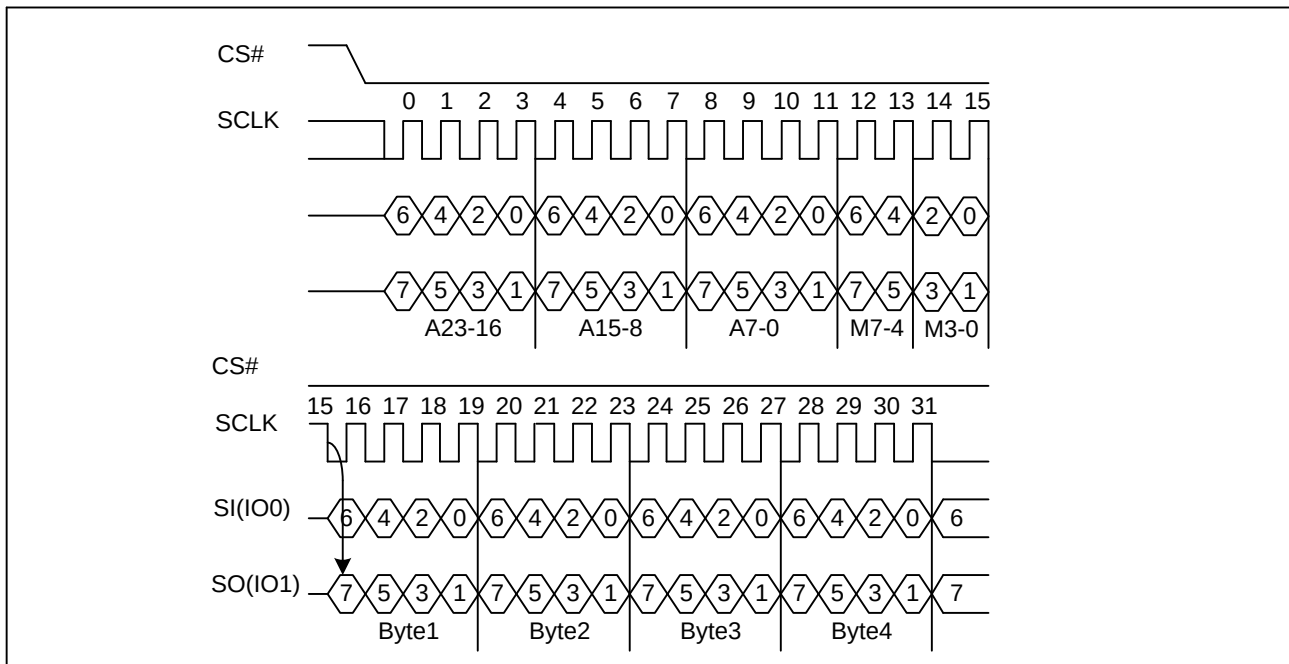




Figure 24 Dual I/O Fast Read Sequence Diagram (M5-4# (1, 0), ADS=1)

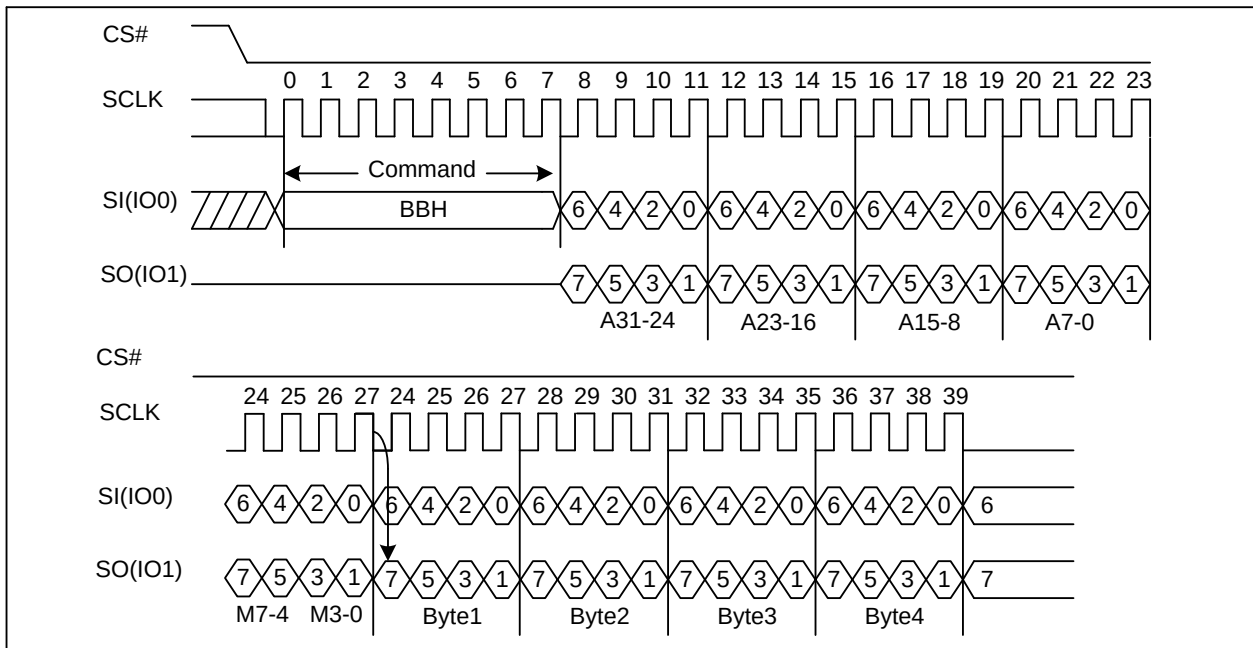


Figure 25 Dual I/O Fast Read Sequence Diagram (M5-4# (1, 0) ADS=1)

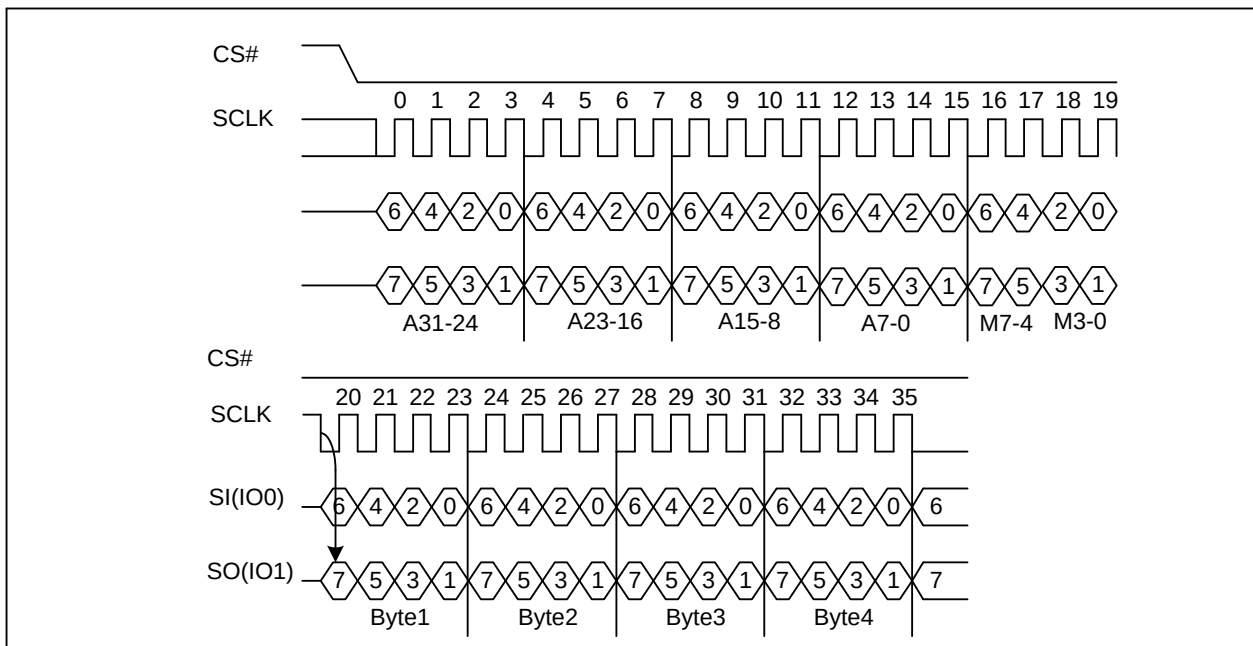




Figure 26 Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4# (1, 0), ADS=0 or ADS=1)

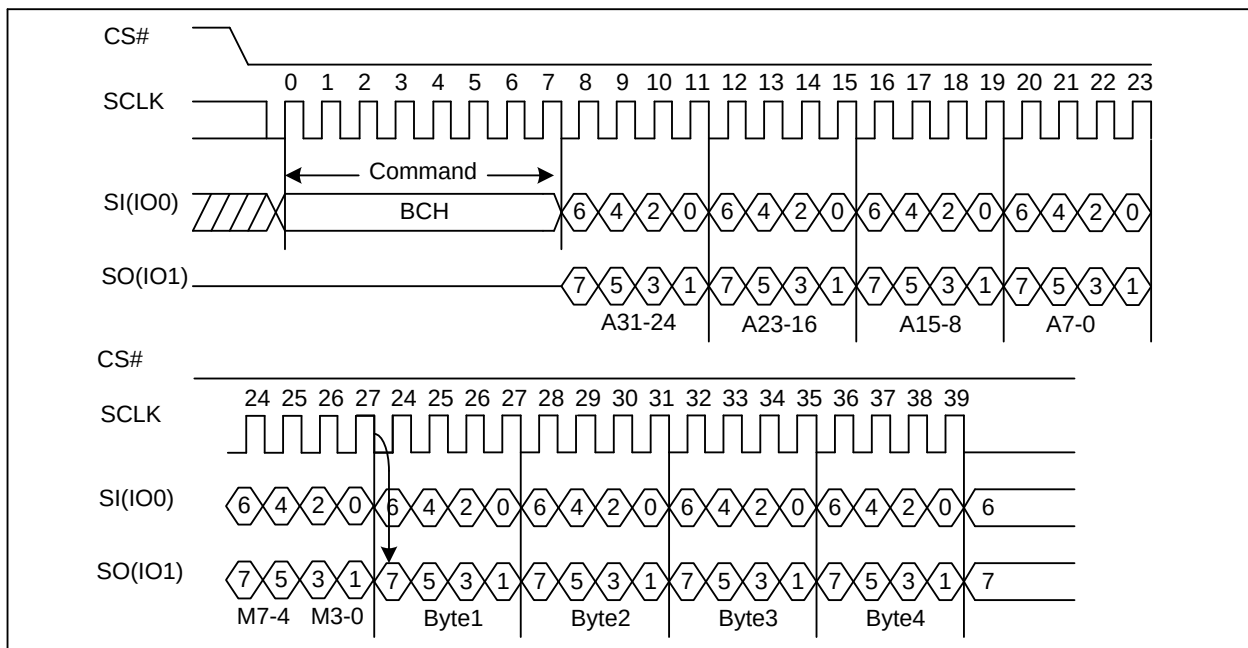
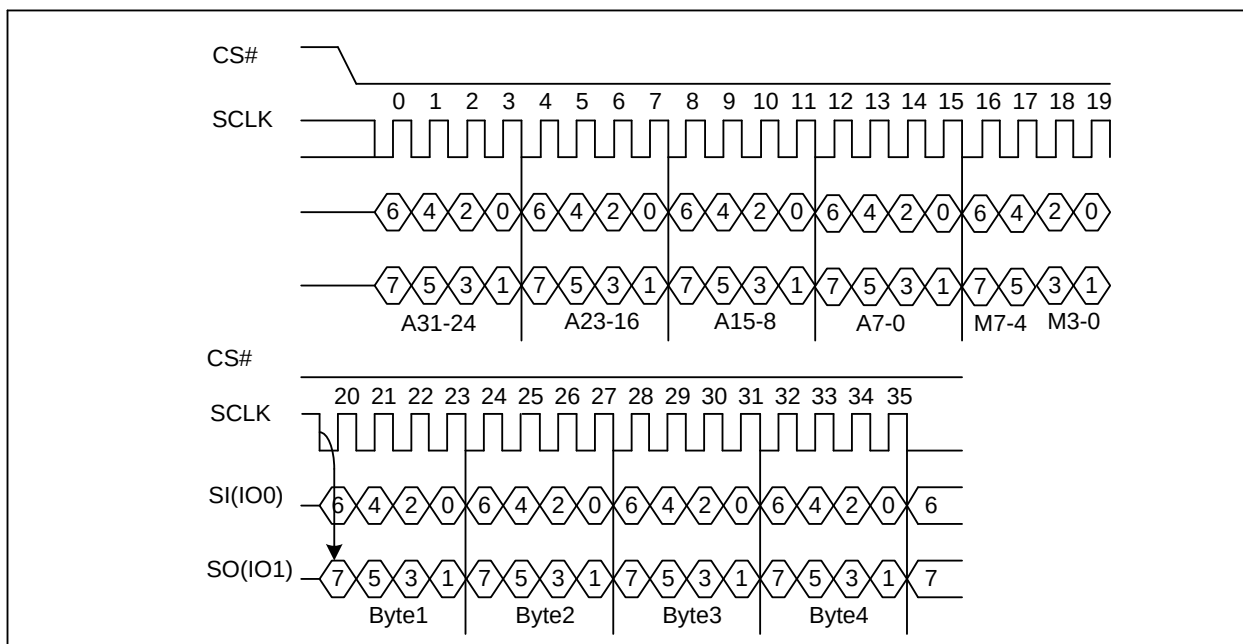


Figure 27 Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4# (1, 0) ADS=0 or ADS=1)





7.13. Quad I/O Fast Read (QIOFR EBH or 4QIOFR ECH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-Byte address (A23-0) and a “Continuous Read Mode” Byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-Byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.

Figure 28 Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=0)

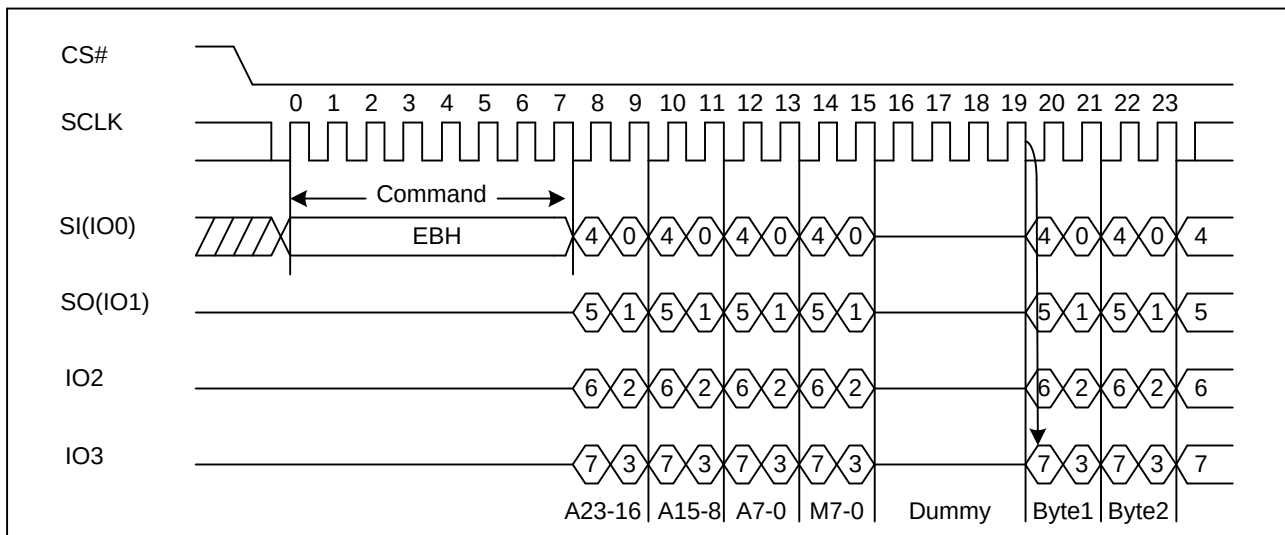




Figure 29 Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=0)

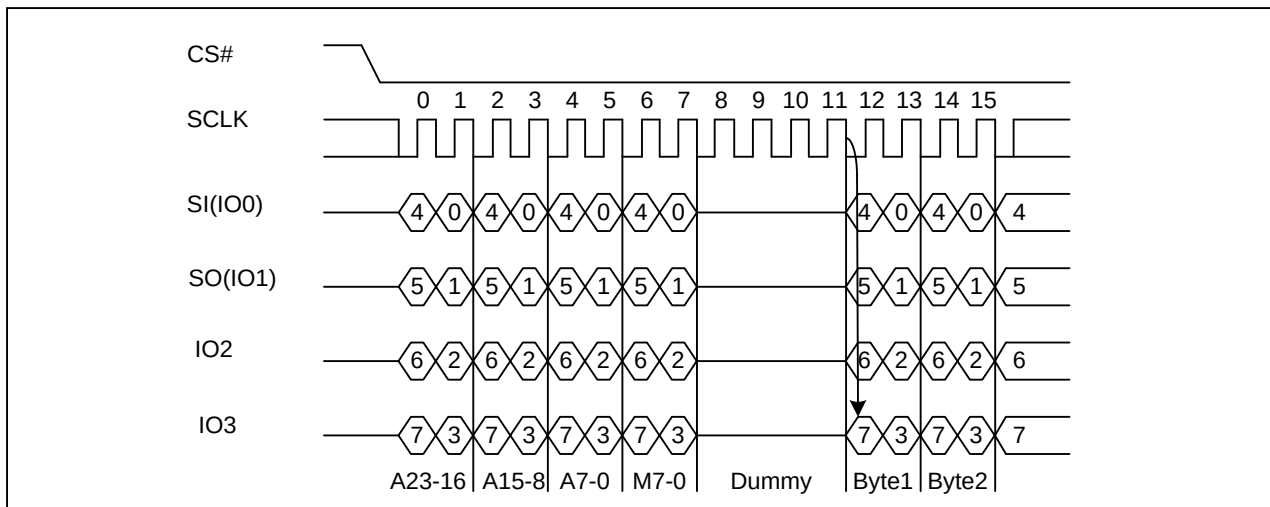


Figure 30 Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=1)

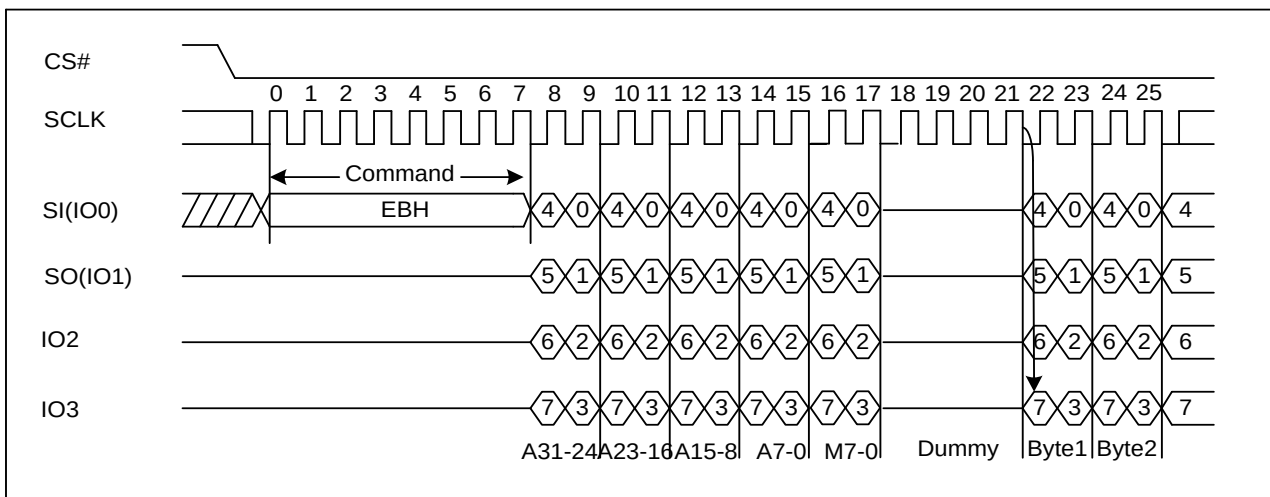




Figure 31 Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=1)

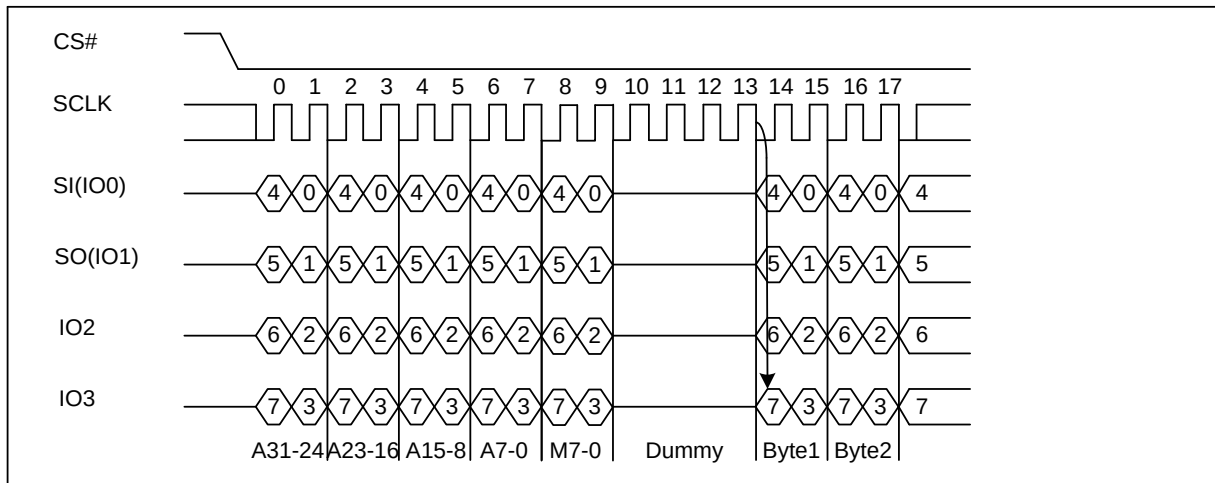


Figure 32 Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4≠ (1, 0), ADS=0 or ADS=1)

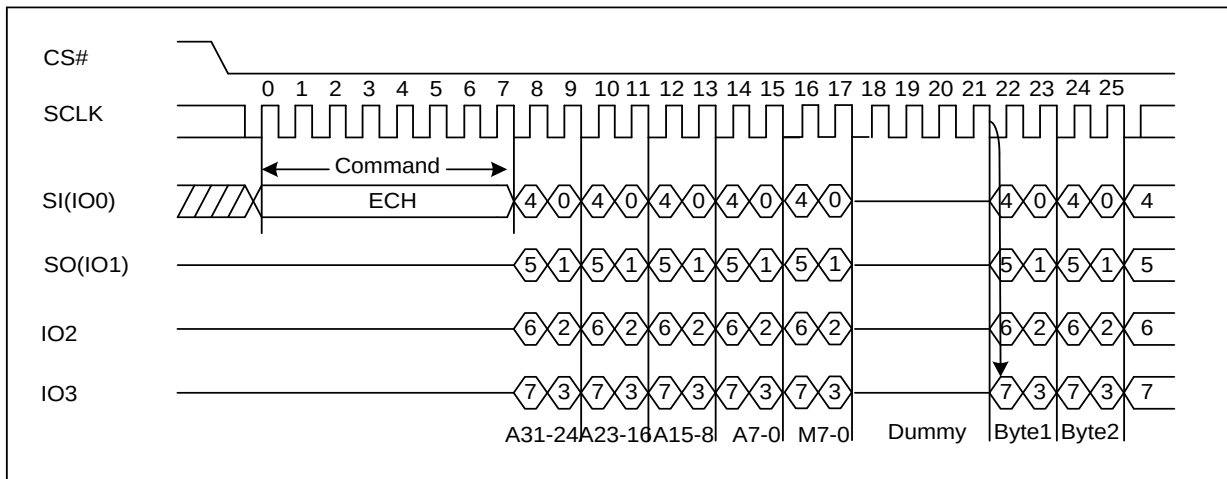
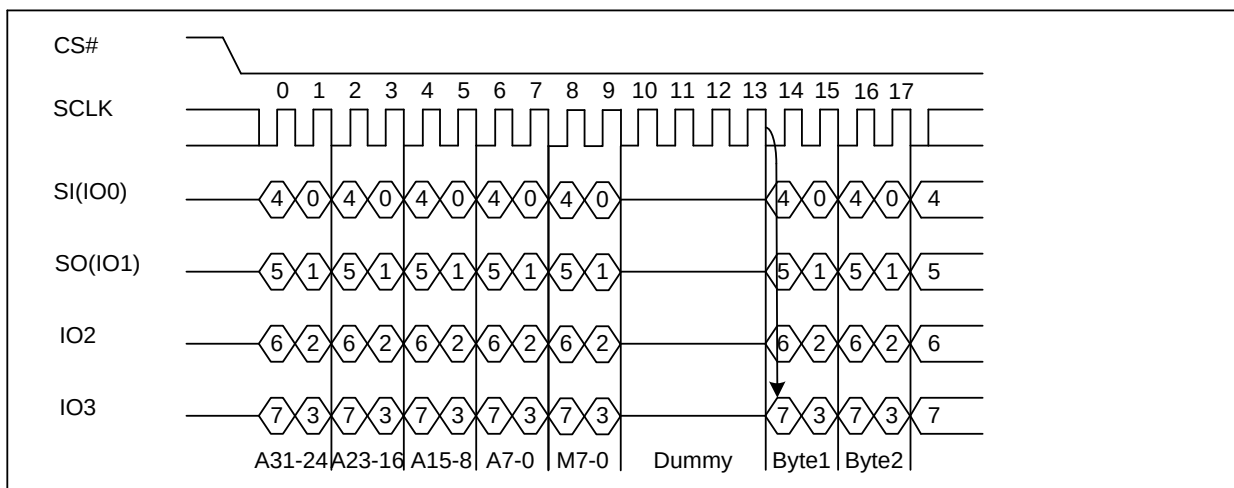


Figure 33 Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4= (1, 0), ADS=0 or ADS=1)





Quad I/O Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to EBH or ECH. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following EBH or ECH commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-Byte section of a 256-Byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-Byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-Byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.14. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read” command to access a fixed length of 8/16/32/64-Byte section within a 256-Byte page, in standard SPI mode.

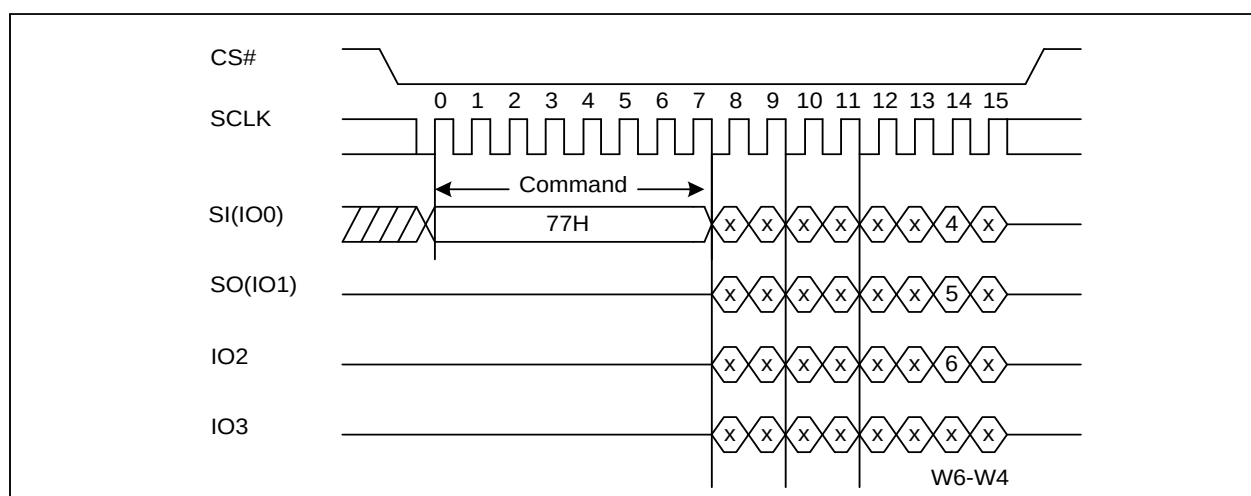
The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits “Wrap bits” → CS# goes high.

Table 16 Set Burst with Wrap configuration

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-Byte	No	N/A
0, 1	Yes	16-Byte	No	N/A
1, 0	Yes	32-Byte	No	N/A
1, 1	Yes	64-Byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read” command will use the W6-W4 setting to access the 8/16/32/64-Byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 34 Set Burst with Wrap Sequence Diagram





7.15. Page Program (PP 02H or 4PP 12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address Bytes and at least one data Byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3 or 4-Byte address on SI → at least 1 Byte data on SI → CS# goes high. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

Figure 35 Page Program Sequence Diagram (ADS=0)

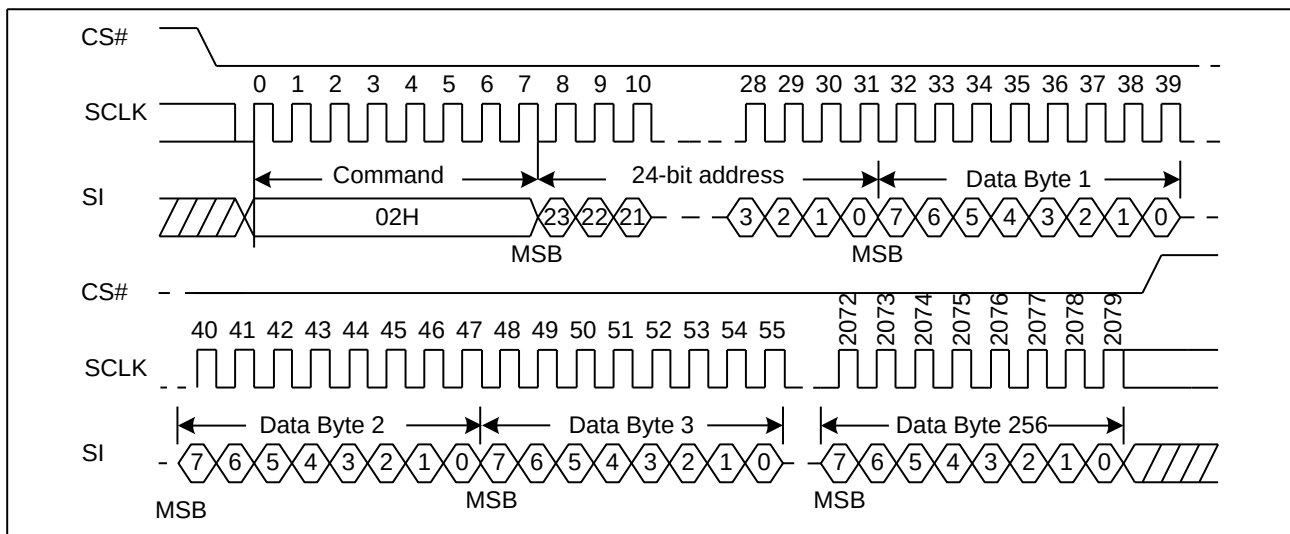




Figure 36 Page Program Sequence Diagram (ADS=1)

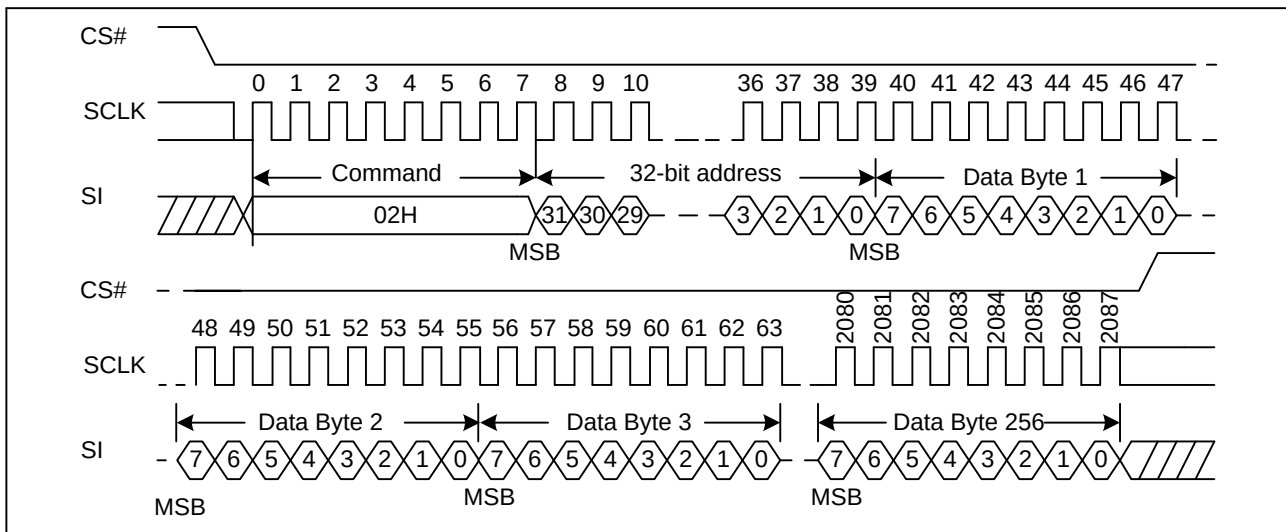
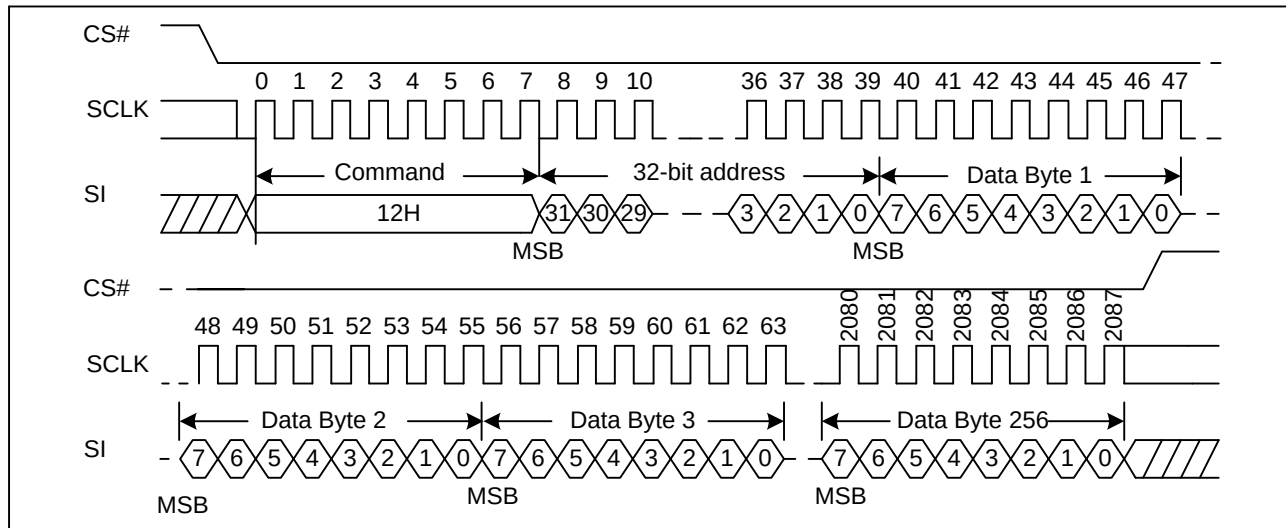


Figure 37 Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.16. Quad Page Program (QPP 32H or 4QPP 34H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address Bytes and at least one data Byte on IO pins.

The command sequence is shown below. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

Figure 38 Quad Page Program Sequence Diagram (ADS=0)

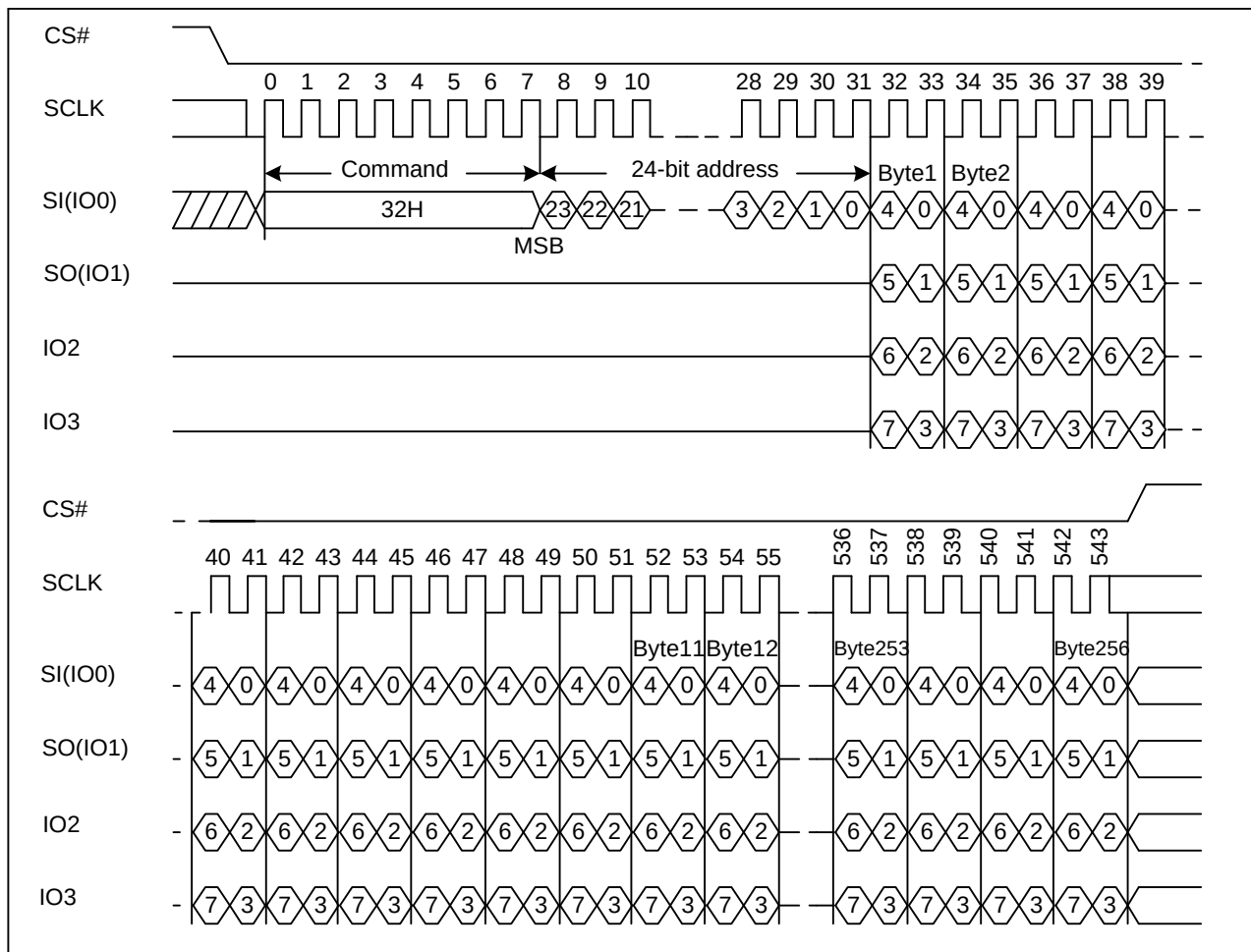


Figure 39 Quad Page Program Sequence Diagram (ADS=1)

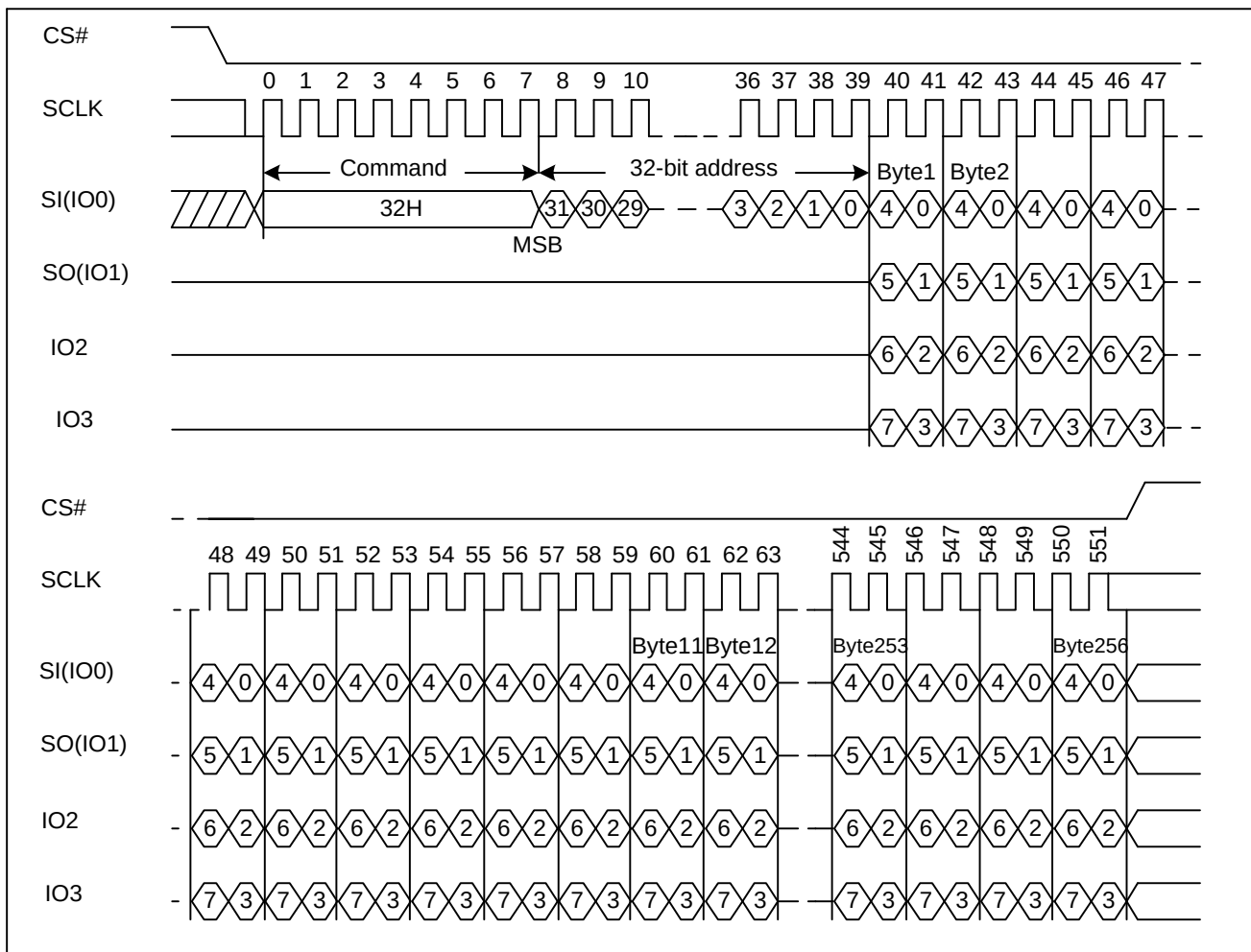
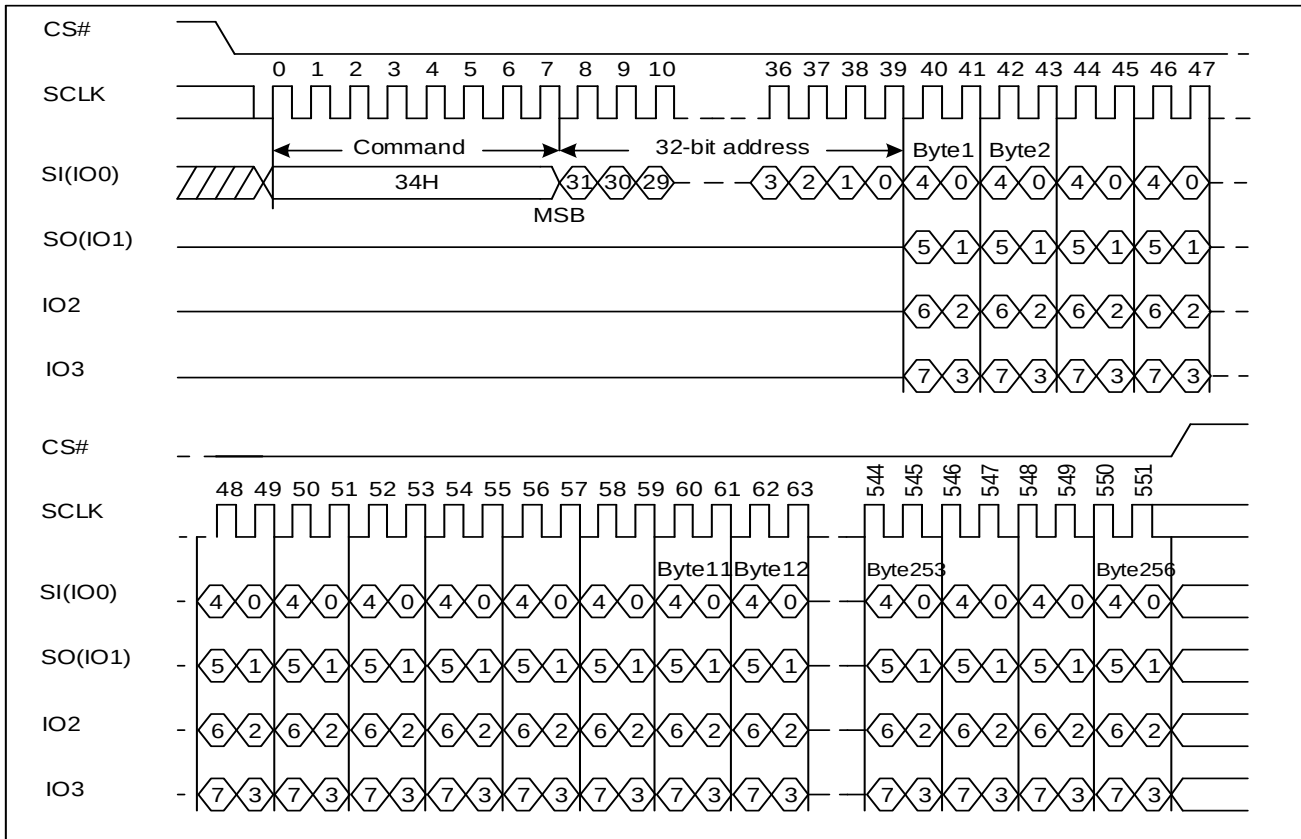




Figure 40 Quad Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.17. Sector Erase (SE 20H or 4SE 21H)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address Byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 41 Sector Erase Sequence Diagram (ADS=0)

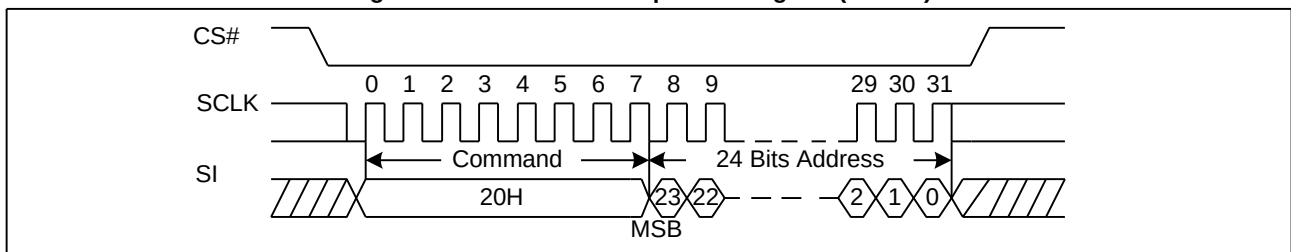


Figure 42 Sector Erase Sequence Diagram (ADS=1)

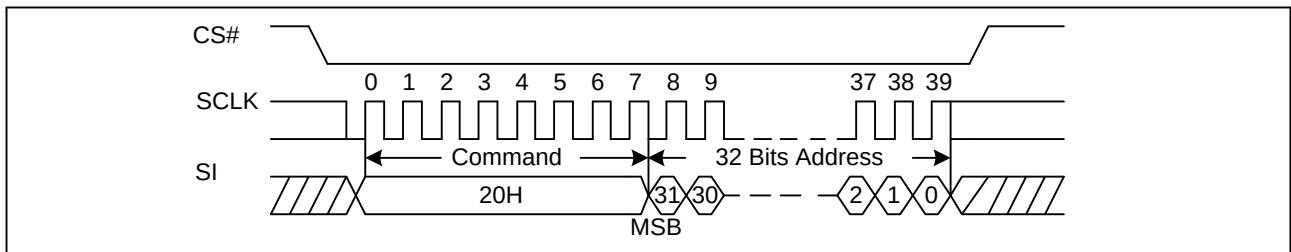
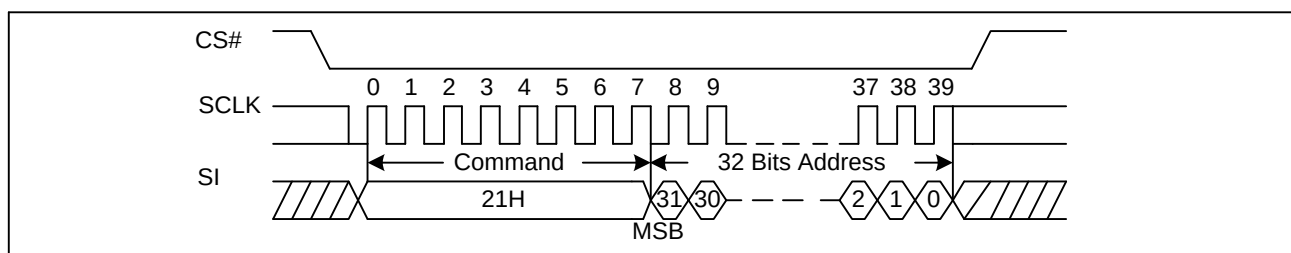


Figure 43 Sector Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.18. 32KB Block Erase (BE32 52H or 4BE32 5CH)

The 32KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address Bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 44 32KB Block Erase Sequence Diagram (ADS=0)

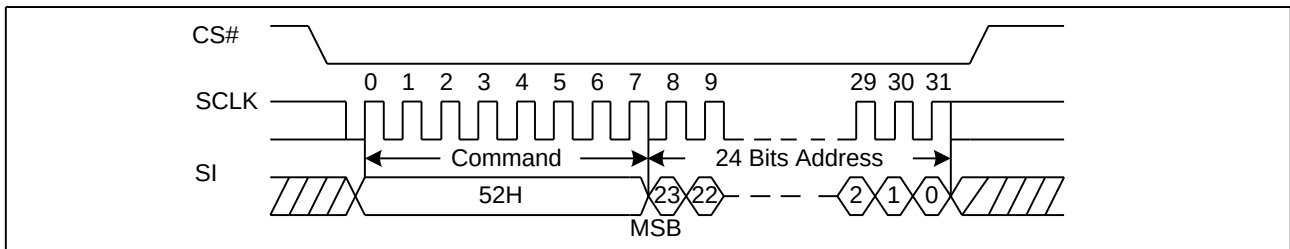


Figure 45 32KB Block Erase Sequence Diagram (ADS=1)

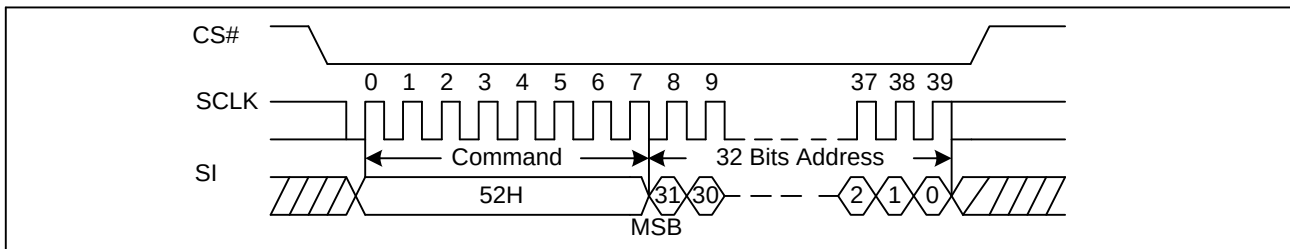
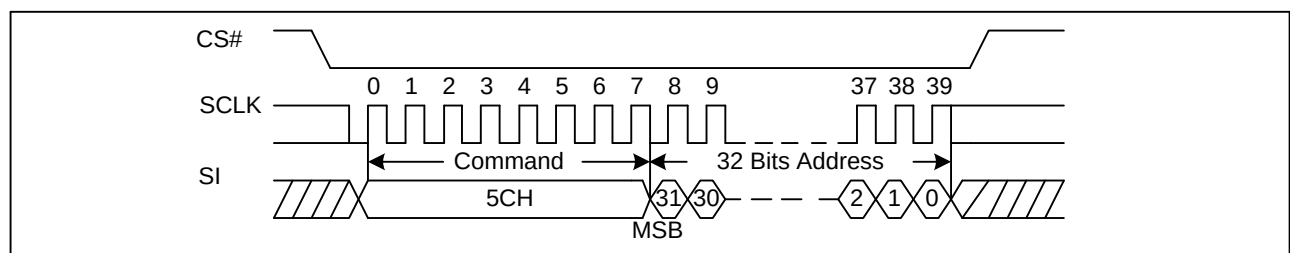


Figure 46 32KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)





7.19. 64KB Block Erase (BE64 D8H or 4BE64 DCH)

The 64KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address Bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 47 64KB Block Erase Sequence Diagram (ADS=0)

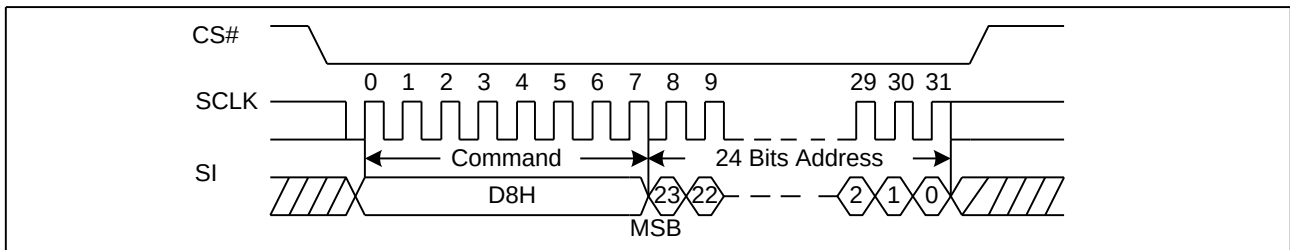


Figure 48 64KB Block Erase Sequence Diagram (ADS=1)

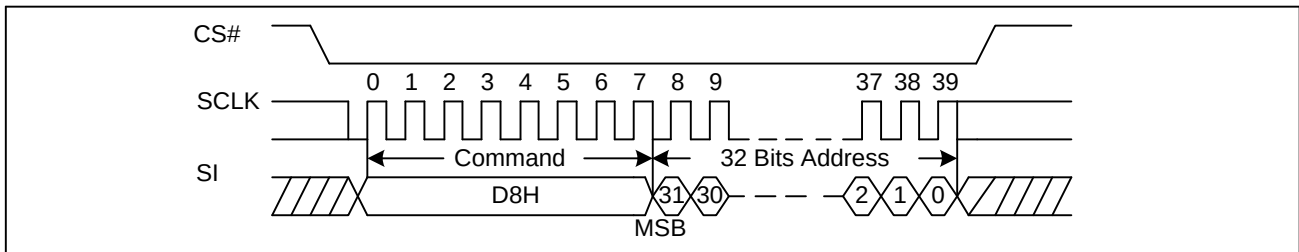
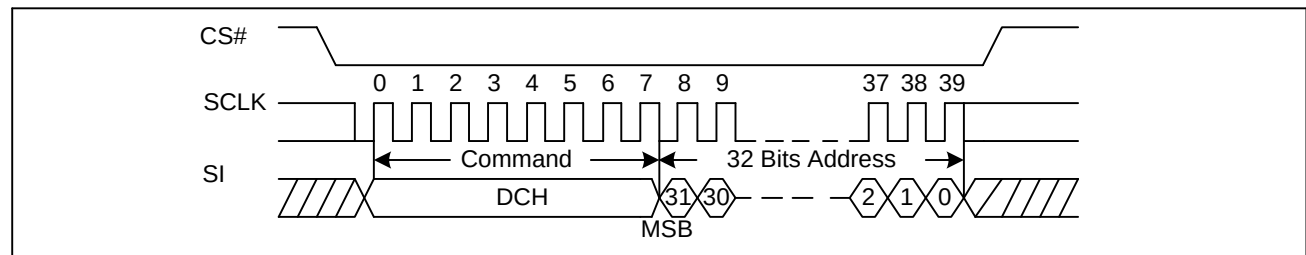


Figure 49 64KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)



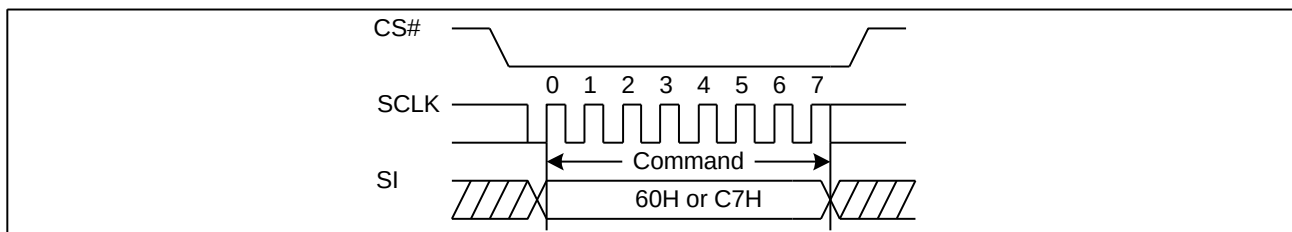


7.20. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors/blocks are protected.

Figure 50 Chip Erase Sequence Diagram





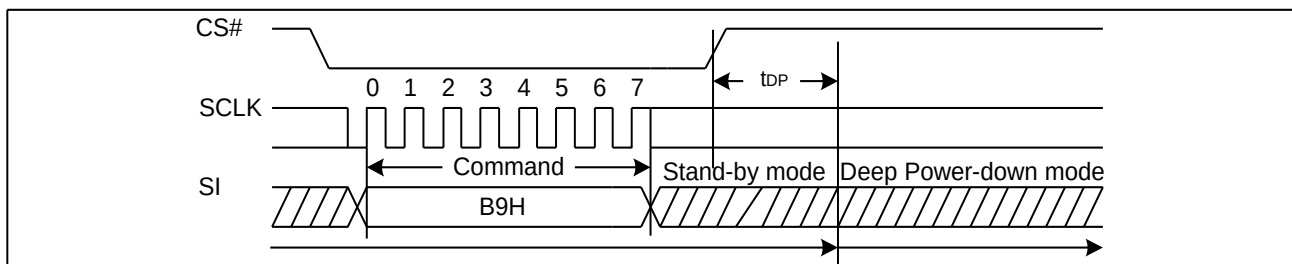
7.21. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Up, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 51 Deep Power-Down Sequence Diagram





7.22. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence in 3 Byte mode (ADS=0): CS# goes low → sending Read Unique ID command → Dummy Byte1 → Dummy Byte2 → Dummy Byte3 → Dummy Byte4 → 128bit Unique ID Out → CS# goes high.

The Read Unique ID command sequence in 4 Byte mode (ADS=0): CS# goes low → sending Read Unique ID command → Dummy Byte1 → Dummy Byte2 → Dummy Byte3 → Dummy Byte4 → Dummy Byte5 → 128bit Unique ID Out → CS# goes high.

Figure 52 Read Unique ID Sequence Diagram (ADS=0)

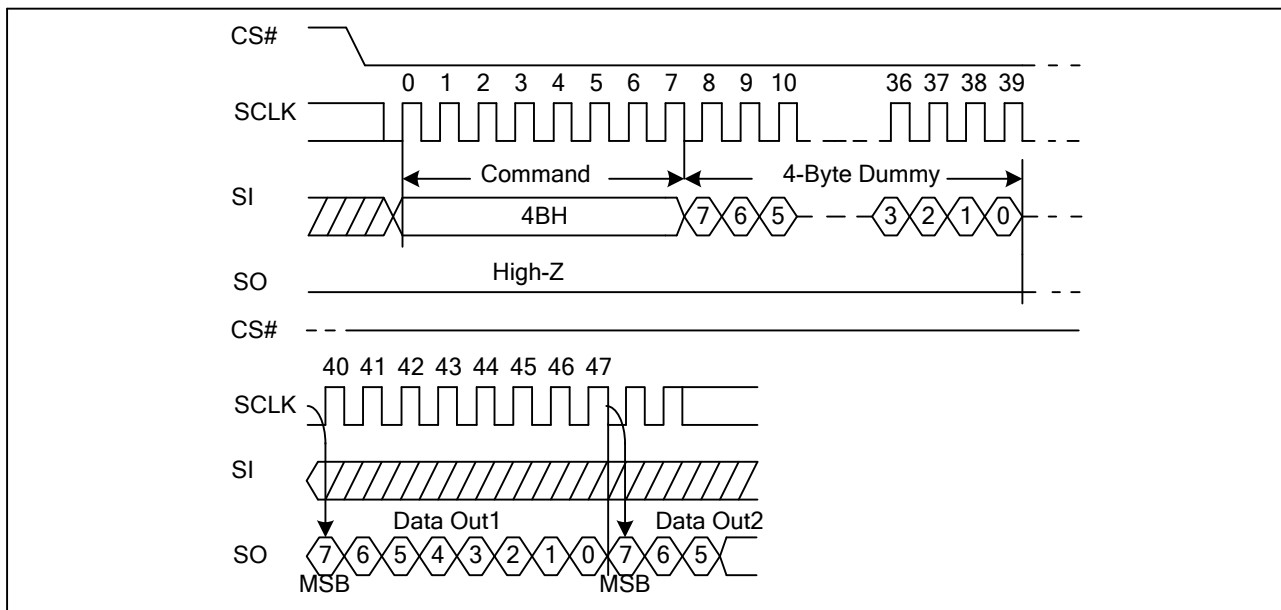
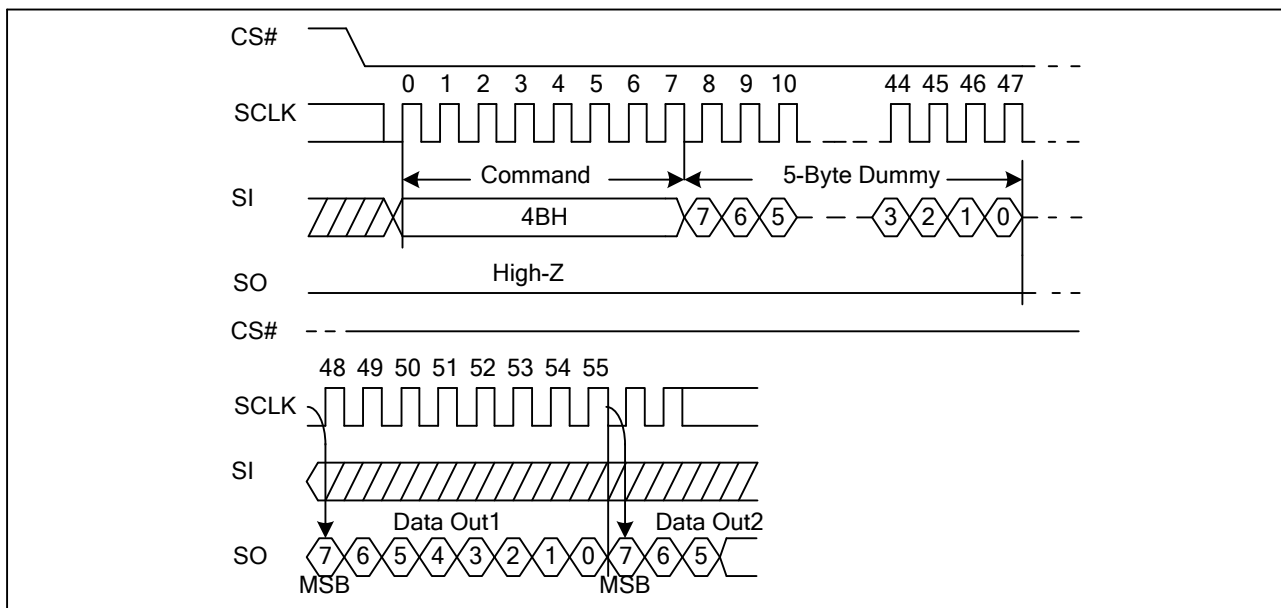


Figure 53 Read Unique ID Sequence Diagram (ADS=1)





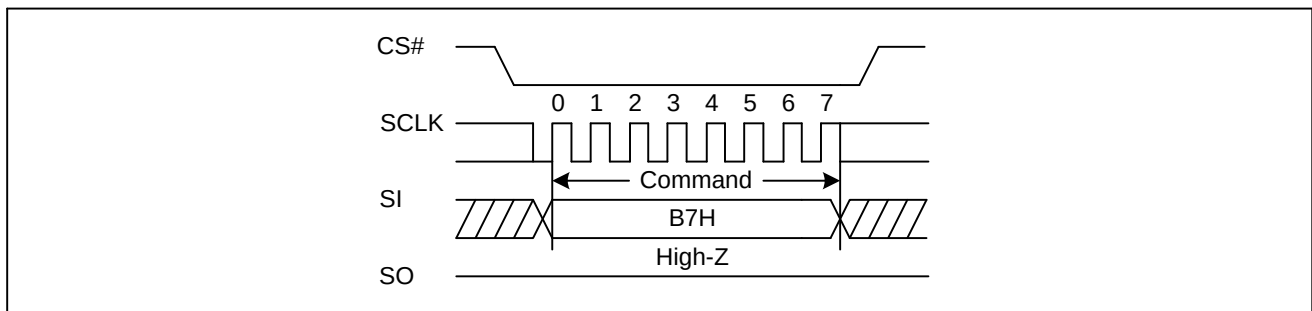
7.23. Enter 4-Byte Address Mode (B7H)

The Enter 4-Byte Address Mode command enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit8 (ADS bit) of status register will be automatically set to “1” to indicate the 4-Byte address mode has been enabled. Once the 4-Byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Enter 4-Byte mode command → CS# goes high.

Figure 54 Enter 4-Byte Address Mode Sequence Diagram

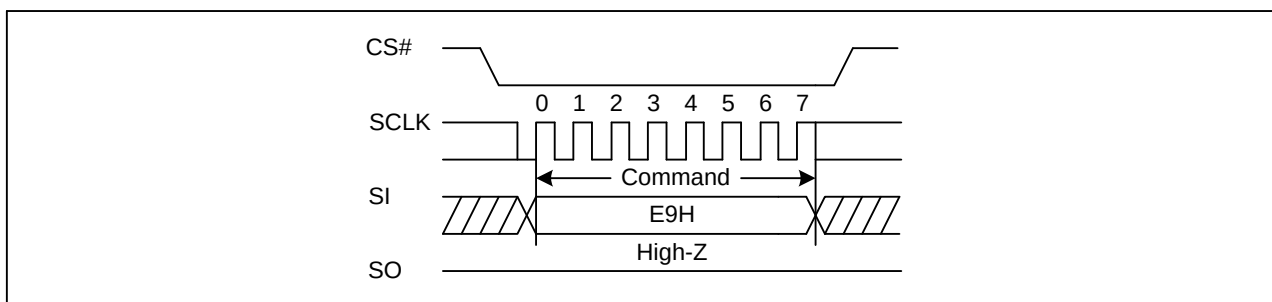


7.24. Exit 4-Byte Address Mode (E9H)

The Exit 4-Byte Address Mode command is executed to exit the 4-Byte address mode and return to the default 3-Byte address mode. After sending out the EX4B instruction, the bit8 (ADS bit) of status register will be cleared to “0” to indicate the exit of the 4-Byte address mode. Once exiting the 4-Byte address mode, the address length will return to 24-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Exit 4-Byte Address Mode command → CS# goes high.

Figure 55 Exit 4-Byte Address Mode Sequence Diagram

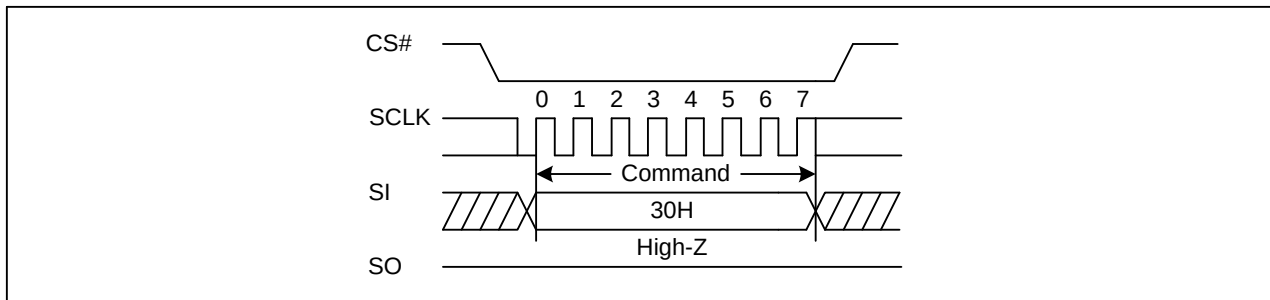




7.25. Clear SR Flags (30H)

The Clear Status Register Flags command resets bit S18 (Program Error bit) and S19 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will not be accepted when the device remains busy with WIP set to 1. The WEL bit will be unchanged after this command is executed.

Figure 56 Clear Status Register Flags Sequence Diagram



7.26. Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown below. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy Byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 57 Release Power-Down Sequence Diagram

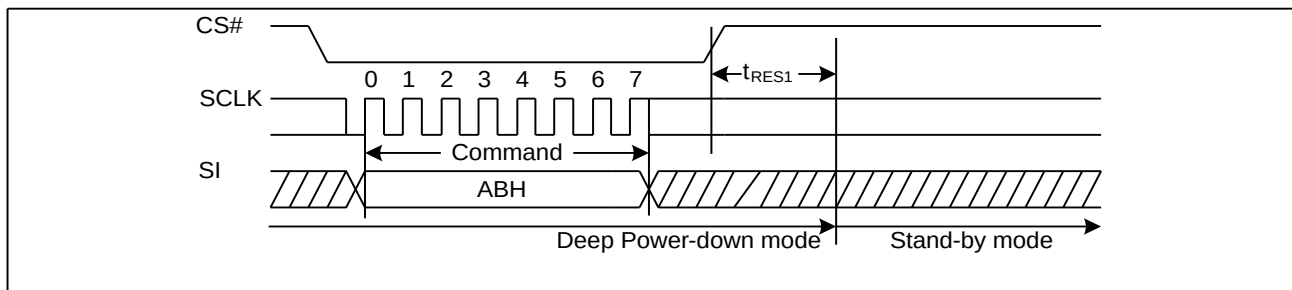
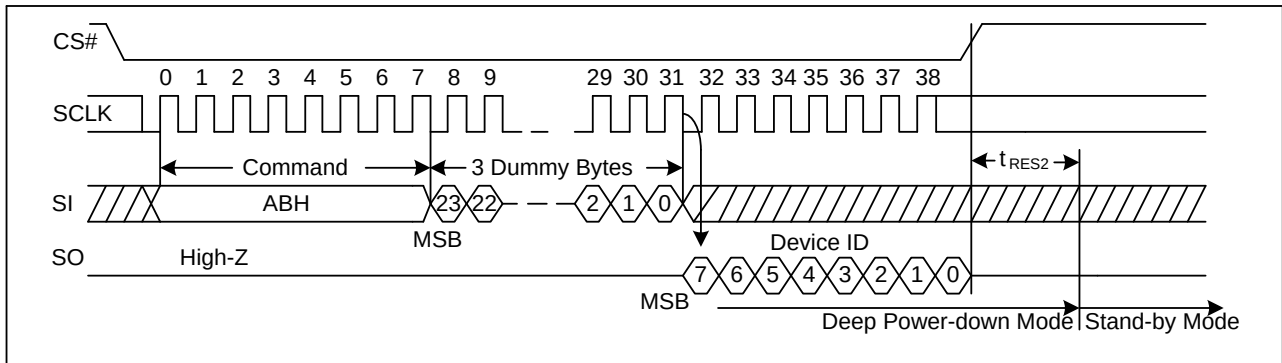




Figure 58 Release Power-Down/Read Device ID Sequence Diagram

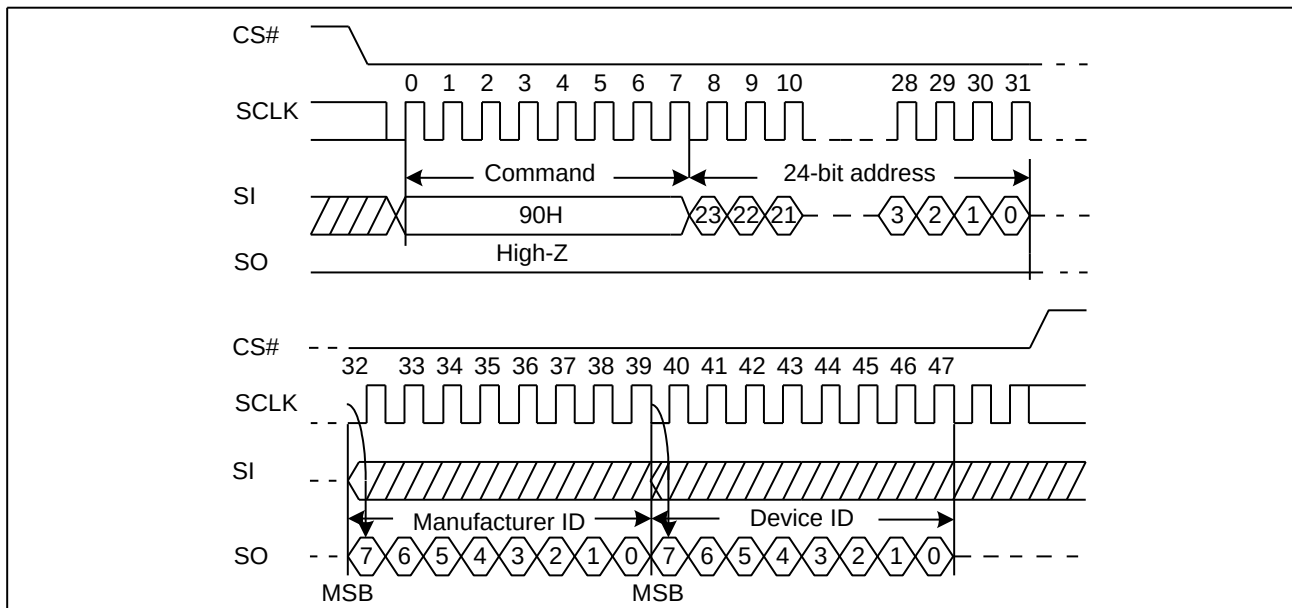


7.27. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 59 Read Manufacture ID/ Device ID Sequence Diagram



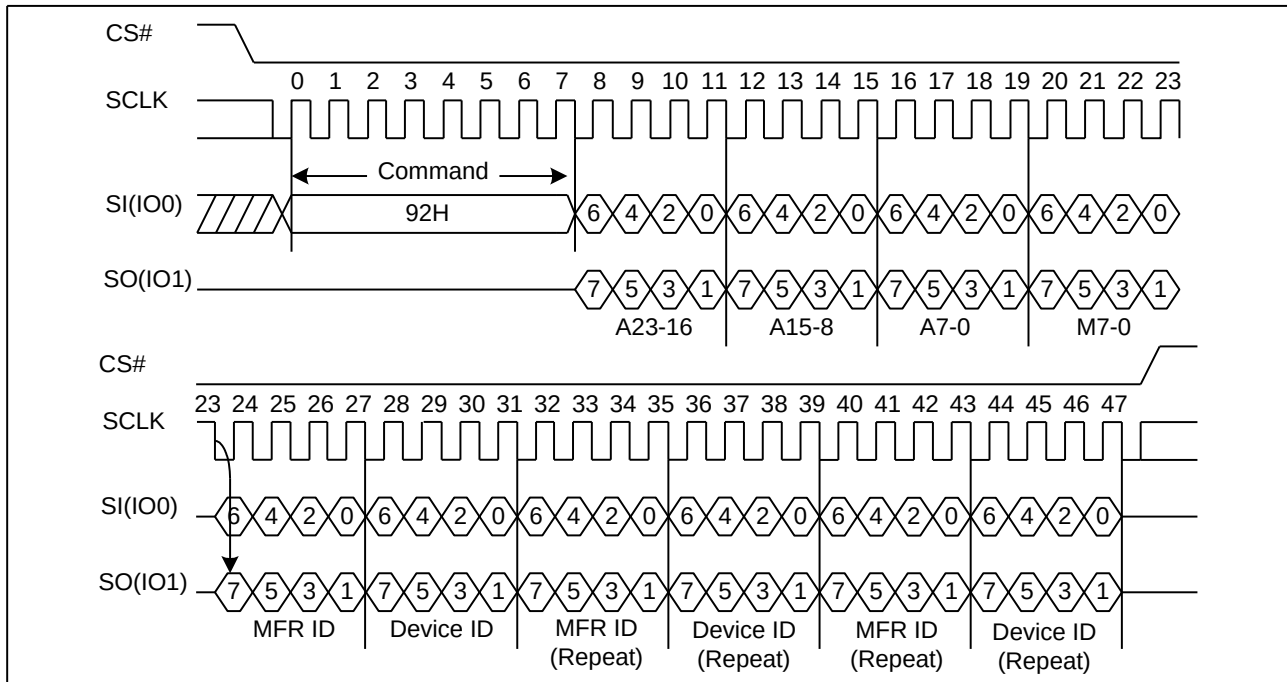


7.28. Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 60. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 60. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram



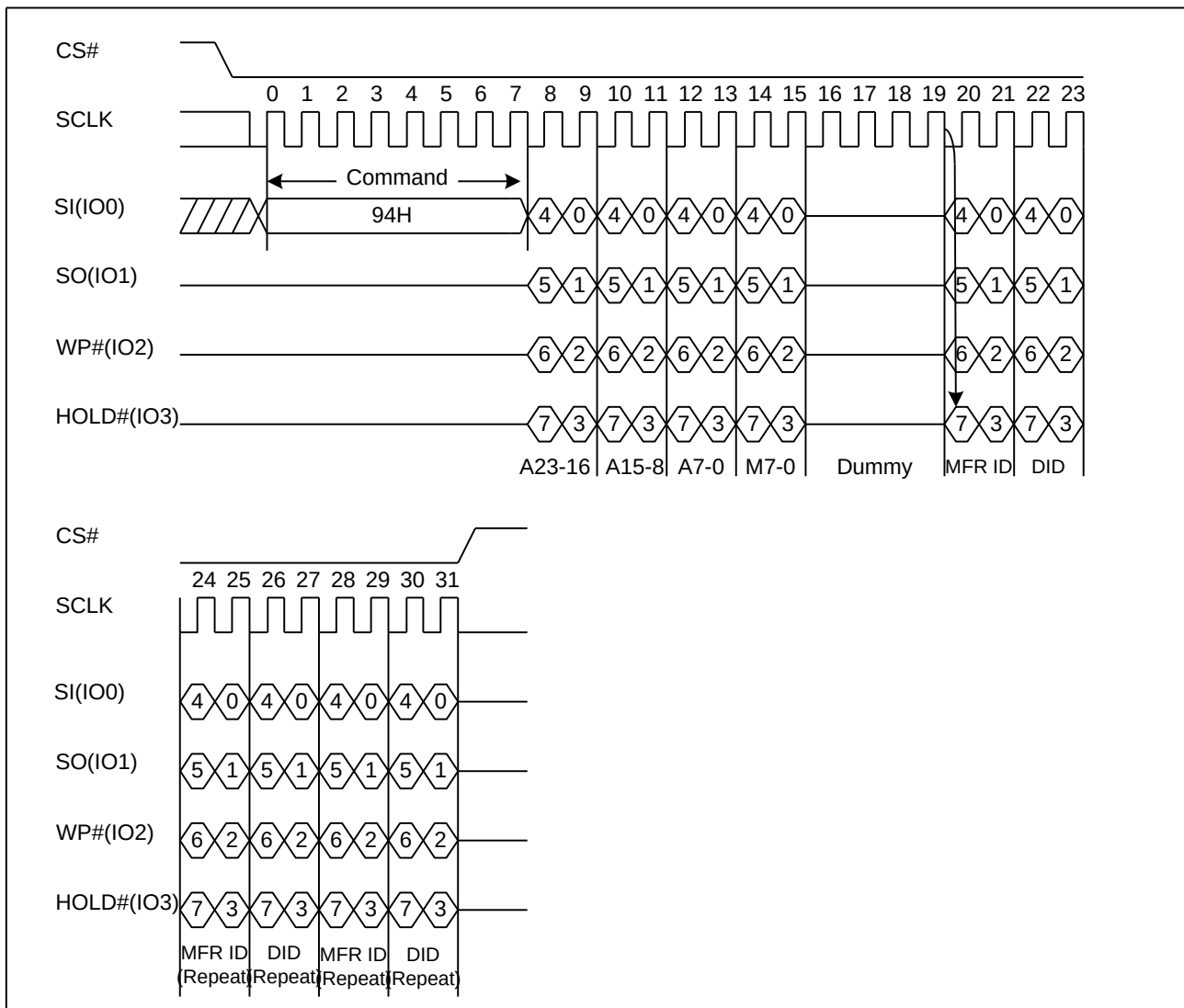


7.29. Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code “94H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 61. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 61. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram



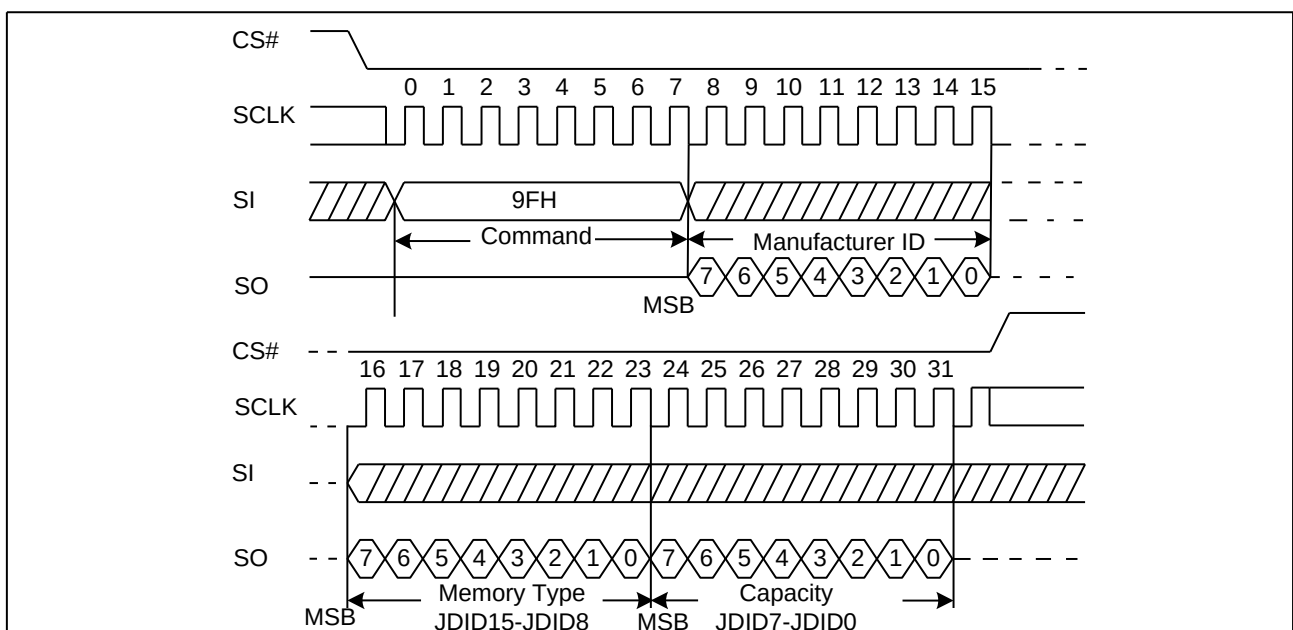


7.30. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two Bytes of device identification. The device identification indicates the memory type in the first Byte, and the memory capacity of the device in the second Byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 62 Read Identification ID Sequence Diagram





7.31. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H/31H/11H) and Erase/Program Security Registers command (44H,42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program suspend. The Write Status Register command (01H/31H/11H) and Erase Security Registers command (44H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

Table 17 Commands Allowed During Program or Erase Suspend

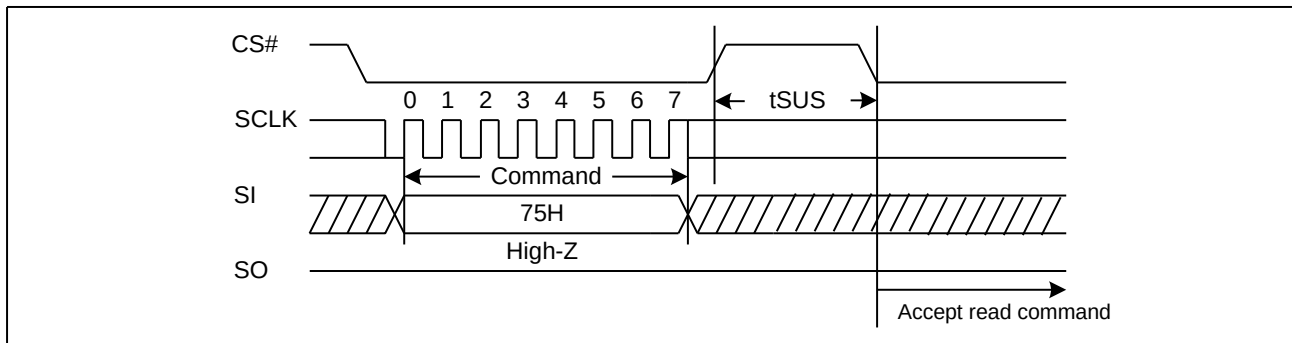
Command Name	Code (Hex)	Allowed During Erase Suspend	Allowed During Program Suspend	Comment
Write Enable	06	Yes		Required for program command within erase suspend.
Read Status Register-1	05	Yes	Yes	Needed to read WIP to determine end of suspend process.
Read Status Register-2	35	Yes	Yes	Needed to read suspend status to determine whether the operation is suspended or complete.
Read Status Register-3	15	Yes	Yes	Needed to read suspend status to determine whether the operation is suspended or complete.
Read Extended Addr. Register	C8	Yes	Yes	Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program.
Write Extended Addr. Register	C5	Yes	Yes	Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program.
Read	03	Yes	Yes	All array reads allowed in suspend.
4Read	13	Yes	Yes	All array reads allowed in suspend.
Fast Read	0B	Yes	Yes	All array reads allowed in suspend.
4Fast Read	0C	Yes	Yes	All array reads allowed in suspend.
Dual I/O Fast Read	BB	Yes	Yes	All array reads allowed in suspend.
4Dual I/O Fast Read	BC	Yes	Yes	All array reads allowed in suspend.
Dual Output Fast Read	3B	Yes	Yes	All array reads allowed in suspend.
4Dual Output Fast Read	3C	Yes	Yes	All array reads allowed in suspend.
Quad I/O Fast Read	EB	Yes	Yes	All array reads allowed in suspend.
4Quad I/O Fast Read	EC	Yes	Yes	All array reads allowed in suspend.
Quad Output Fast Read	6B	Yes	Yes	All array reads allowed in suspend.
4Quad Output Fast Read	6C	Yes	Yes	All array reads allowed in suspend.
Page Program	02	Yes		Required for array program during erase suspend.
4Page Program	12	Yes		Required for array program during erase suspend.
Quad Page Program	32	Yes		Required for array program during erase suspend.
4Quad Page Program	34	Yes		Required for array program during erase suspend.
Program/Erase Resume	7A	Yes		Required to resume from erase/program suspend.



Enable Reset	66	Yes	Yes	Reset allowed anytime.
Reset	99	Yes	Yes	Reset allowed anytime.

The Program/Erase Suspend command will be accepted by the device only if the SUS2/SUS1 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS2/SUS1 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS2/SUS1 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

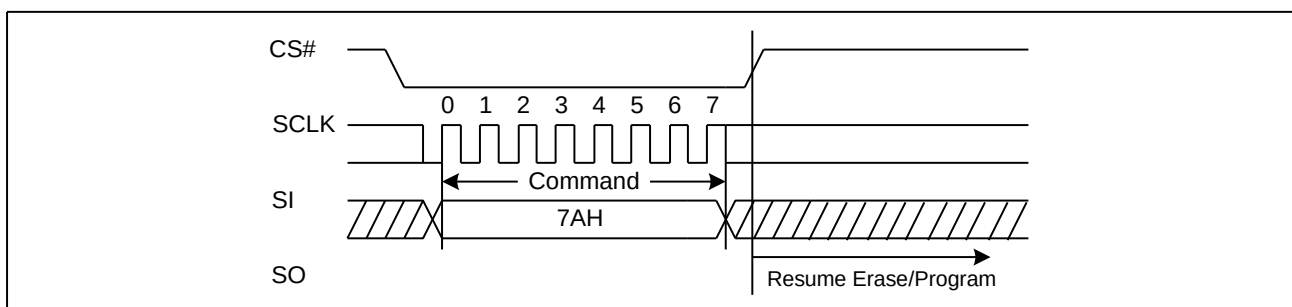
Figure 63 Program/Erase Suspend Sequence Diagram



7.32. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS2/SUS1 bit equal to 1 and the WIP bit equal to 0. After issued the SUS2/SUS1 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 64 Program/Erase Resume Sequence Diagram





7.33. Erase Security Registers (44H)

The GD25R256D provides three 2048-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3 or 4-Byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Table 18 Security Registers

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0 0 0 1	0	Do not care
Security Register #2	00H	0 0 1 0	0	Do not care
Security Register #3	00H	0 0 1 1	0	Do not care

Figure 65 Erase Security Registers command Sequence Diagram (ADS=0)

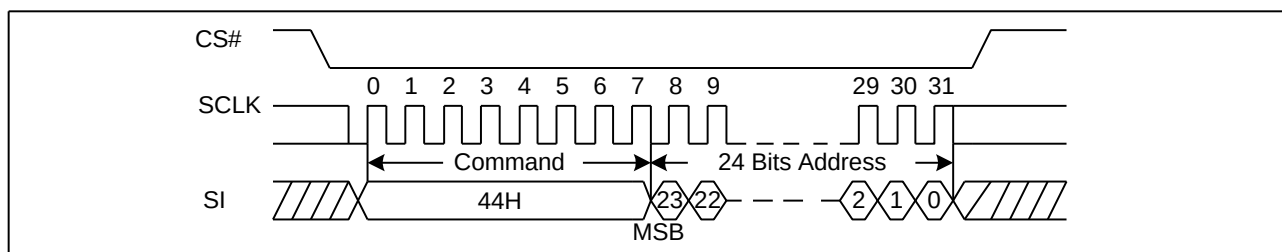
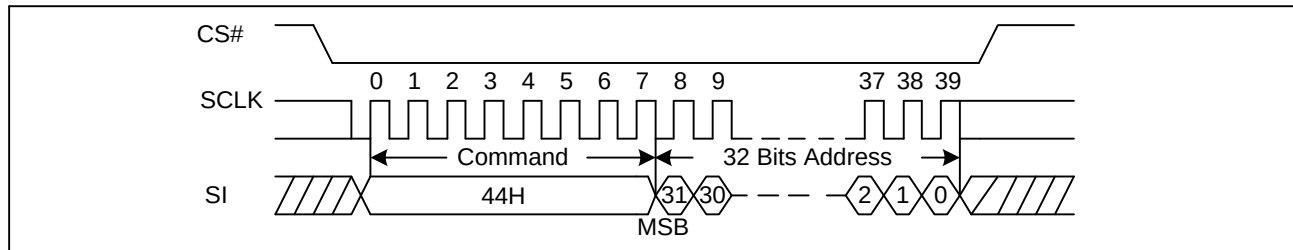


Figure 66 Erase Security Registers command Sequence Diagram (ADS=1)





7.34. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address Bytes and at least one data Byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Table 19 Security Registers

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0 0 0 1	0	Byte Address
Security Register #2	00H	0 0 1 0	0	Byte Address
Security Register #3	00H	0 0 1 1	0	Byte Address

Figure 67 Program Security Registers command Sequence Diagram (ADS=0)

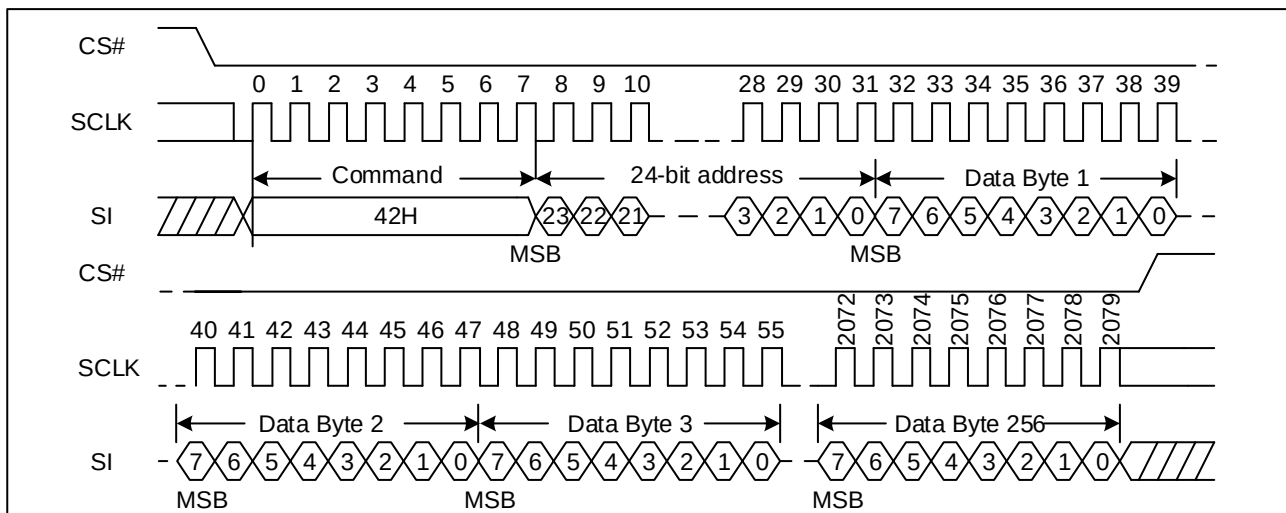
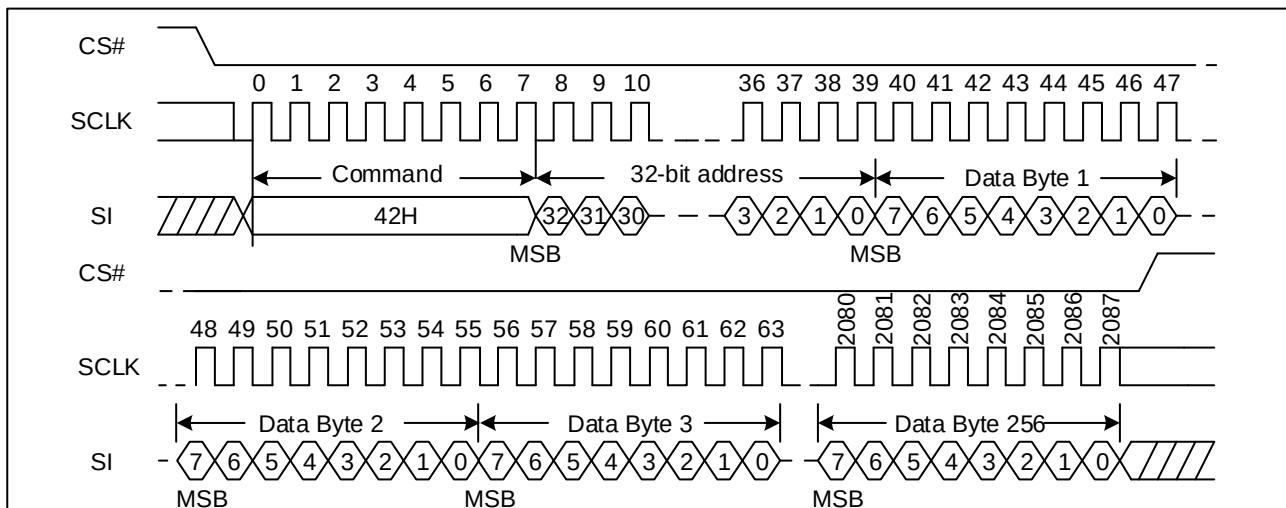


Figure 68 Program Security Registers command Sequence Diagram (ADS=1)





7.35. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command I is followed by a 3-Byte address (A23-A0) or 4-Byte address (A31-A0) and a dummy Byte, and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency f_c , on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. Once the A10-A0 address reaches the last Byte of the register (Byte 7FFH), it will reset to 000H, the command is completed by driving CS# high.

Table 20 Security Registers

Address	A23-16	A15-12	A11	A10-0
Security Register #1	00H	0 0 0 1	0	Byte Address
Security Register #2	00H	0 0 1 0	0	Byte Address
Security Register #3	00H	0 0 1 1	0	Byte Address

Figure 69 Read Security Registers command Sequence Diagram (ADS=0)

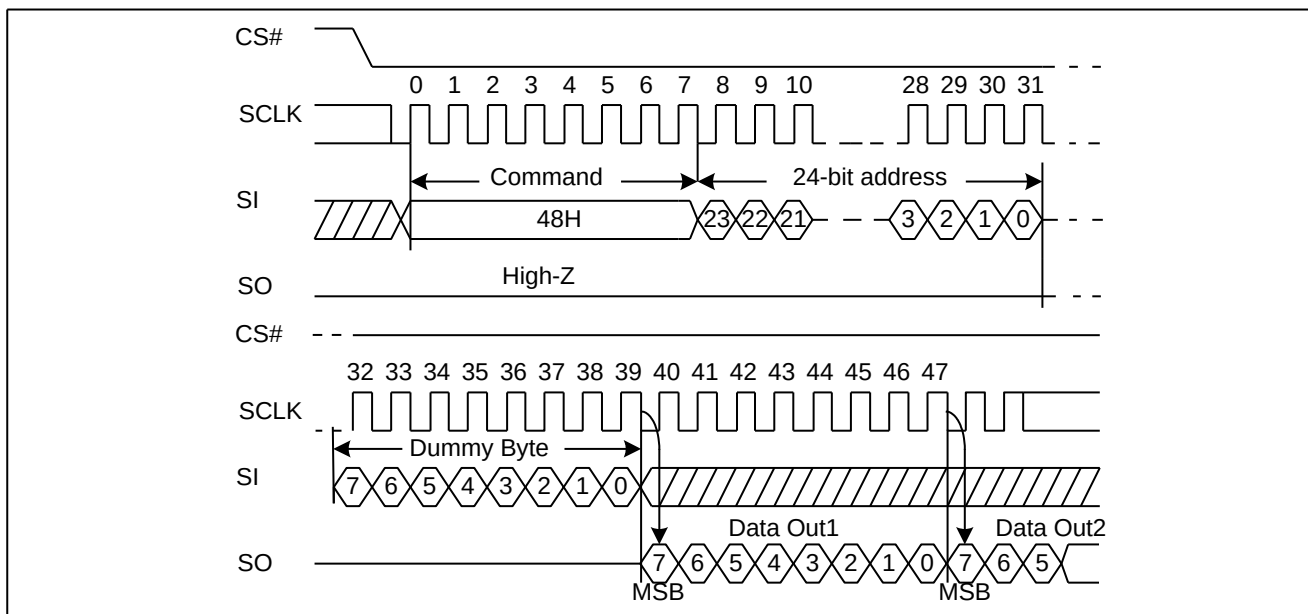
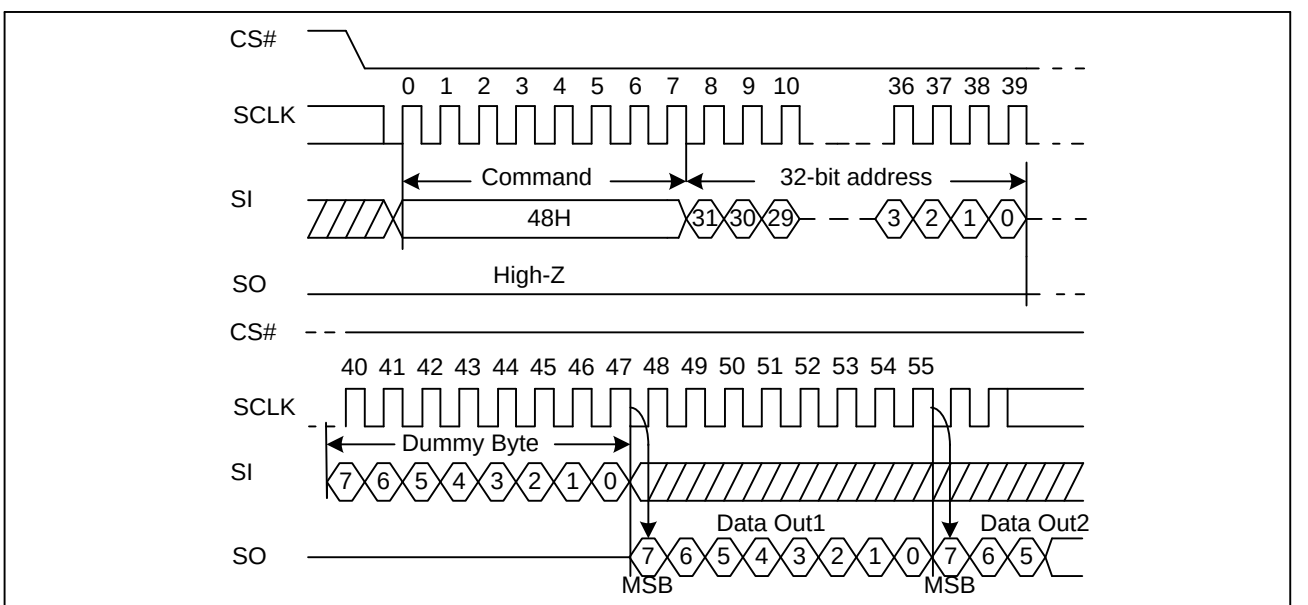


Figure 70 Read Security Registers command Sequence Diagram (ADS=1)



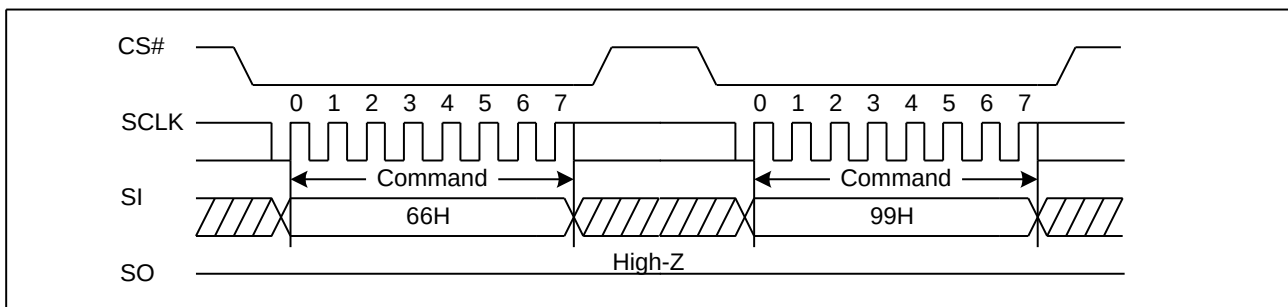


7.36. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in SPI mode. The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST} / t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 71 Enable Reset and Reset command Sequence Diagram



7.37. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure 72 Read Serial Flash Discoverable Parameter command Sequence Diagram

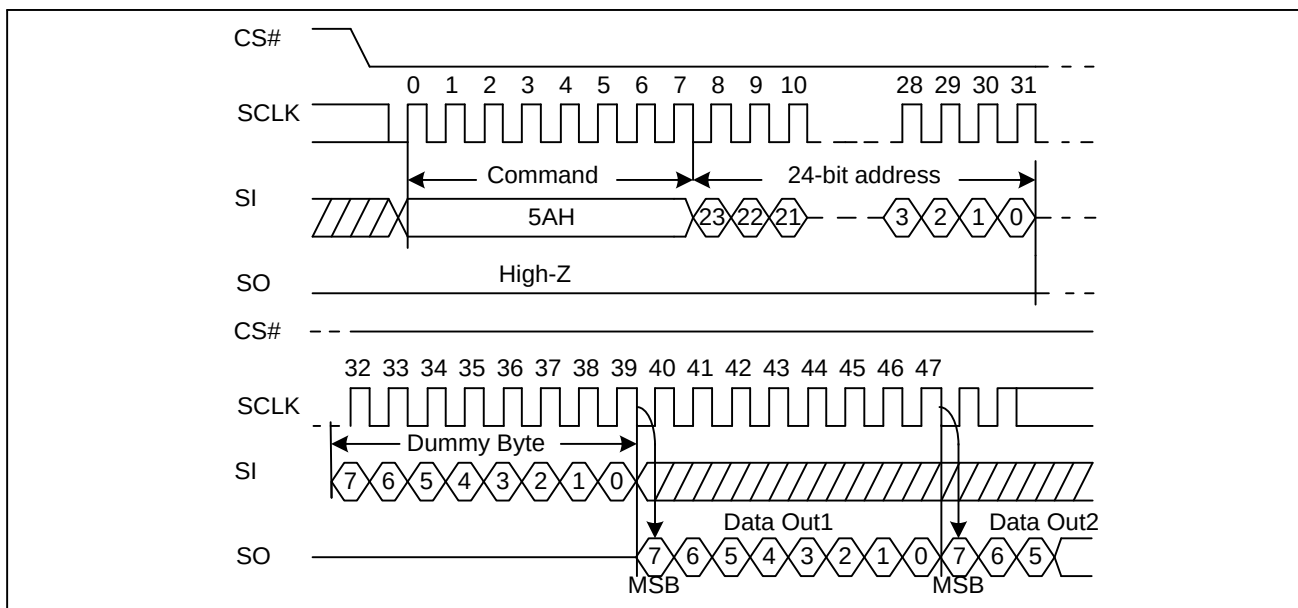


Table 7. Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)



8. RPMC COMMANDS DESCRIPTION

Table 8. Replay Protected Monotonic Counter (RPMC) Commands

Function	Opcode Phase 8 bits	Payload Phase Max 512 Bits		Comment
		Byte#	Field Description	
Command: Write Root Key Register	OP1	1 2 3 4-35 36-63	CmdType[7:0] = 00H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits RootKey[255:0] = 256 Bits TruncatedSign[223:0] = 224 Bits	OP1 + Payload phase driven by host controller. Root Key Register is written only once.
Command: Update HMAC Key Register	OP1	1 2 3 4-7 8-39	CmdType[7:0] = 01H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits KeyData[31:0] = 32 Bits, Signature[255:0] = 256 Bits	OP1 + Payload phase is Issued by host controller on every power up to initialize HMAC Key Register.
Command: Increment Monotonic Counter	OP1	1 2 3 4-7 8-39	CmdType[7:0] = 02H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits CounterData[31:0] = 32 Bits, Signature[255:0] = 256 Bits	OP1 + Payload Phase is Issued by host controller during runtime to increment the counter.
Command: Request Monotonic Counter	OP1	1 2 3 4-15 16-47	CmdType[7:0] = 03H CounterAddr[7:0] = 8 Bits Reserved[7:0] = 8 Bits Tag [95:0] = 96 Bits Signature[255:0] = 256 Bits	OP1 + Payload Phase is Issued by host controller during runtime to request counter data
Command: Read Data	OP2	2 3-14 15-18 19-50	ExtendedStatus[7:0] = 8 Bits Tag[95:0] = 96 Bits CounterData[31:0] = 32 Bits Signature[255:0] = 256 Bits	OP2 is issued by Host Controller generally after an OP1. SPI Flash device responds with the Payload phase to return Extended Status and counter data.

All individual fields are Byte wide fields. For a multi-byte field, Most Significant Byte is issued first; Least Significant Byte is issued last. Within a Byte, Most Significant Bit is issued first; Least Significant Bit is issued last. CmdType is always the first byte issued after OP1 commands. OP2 delay is the same as Fast Read Command delay which is 8 dummy bits.



Table 9. OP1 and OP2 are defined for 1-1-1 mode.

Byte #	0	1	2	3	4	5	6	...	..	..
Name	OP1	CmdType	Counter Address	As defined in the table above						
Name	OP2	8 Dummy clocks	Extended Status[7:0]	As defined in the table above						

After an OP1 command is received, the SPI Flash will indicate status busy indication using either the status register or extended status register as defined below.

Table 10. Extended Status Register Definition

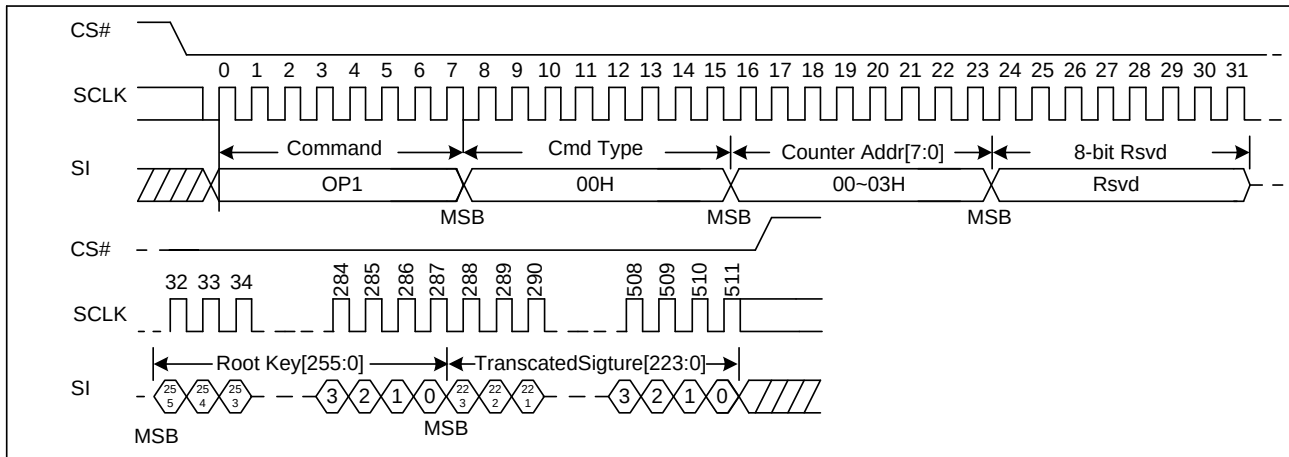
Extended Status[7:0]	Applicable CmdType(s)	Description
00000000	-	Power On State (OP2 issued directly after power-up).
10000000	00,01,02,03,	This status is set on successful completion (no errors) of OP1 command.
0xxxxx1	00,01,02,03, 04-0FF	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxxx1x	00,01	This bit is set only when the correct payload size is received. When cmdtype = 0, this error bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For cmdtype = 01 this bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	00,01,02,03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	02,03	This bit is set on HMAC Key Register or monotonic counter uninitialized on previous OP1 command when correct payload size is received
0xx1xxxx	02	This bit is set on Counter Data Mismatch on previous increment when correct payload size is received
0x1xxxxx	-	Fatal Error. It is set when no valid counter is found after initialization.
Current value		Extended status register will not be updated until first 8 bits of OP1 is received. The correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.

8.1. Command: Write Root Key Register

This command is used to initialize the Root Key Register corresponding to the received Counter Address with the received Root Key. It is suggested to be used in an OEM manufacturing environment when the SPI Flash Controller and SPI Flash are powered together for the first time.



Figure 37. Write Root Key Register Sequence Diagram



Truncated signature field is the same as least significant 224 bits of HMAC-SHA-256 based signature computed based on received input parameters:

- HMAC message[31:0] = (OpCode[7:0], CmdType[7:0], CounterAddr[7:0], Reserved[7:0])
- HMAC Key[255:0] = Root_Key[255:0]

If Root Key != 256'HFF..FF then this command can be executed one time. If the received transaction is error free SPI Flash device successfully executes the command and posts "successful completion" extended status.

Root Key Register Write with root key is = 256'HFF...FF can be used as a temporary key.

If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

Table 11. Expected Extended Status [7:0] results

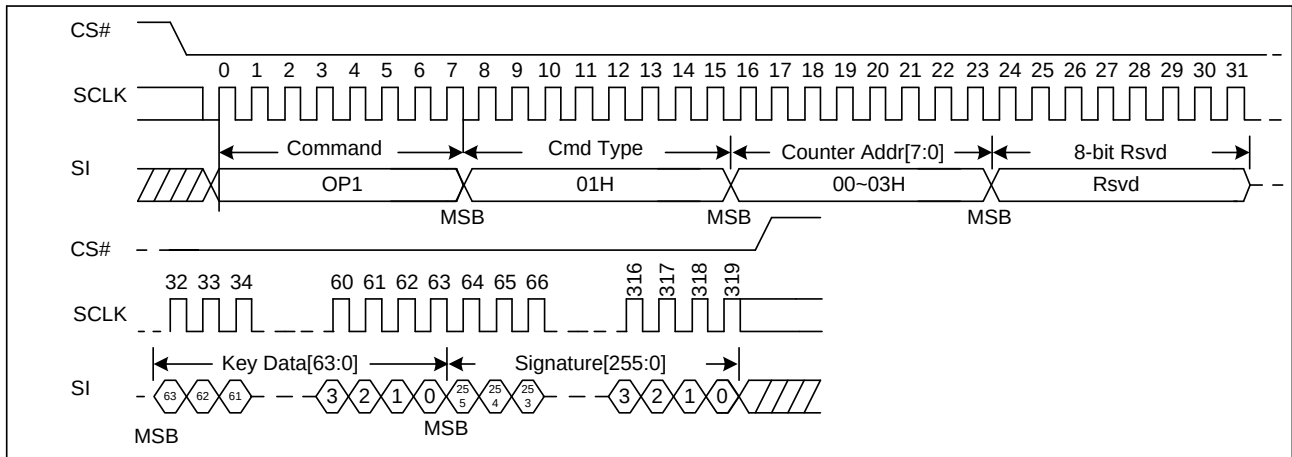
Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	00	Successful completion
0xxxxxx1	00	If Busy_Polling_Method bit in SFDP table is zero, then this bit must be set to 1, when device is busy executing command. It is reset to 0 when OP1 command execution is done. If Busy_Polling_Method bit in SFDP table is one, then this bit is ignored by the controller.
0xxxxx1x	00	This bit is only set when correct payload size is received. It is set on Root Key Register Overwrite or Counter Address is out of range or when there is a truncated signature mismatch error
0xxxx1xx	00	This bit is set when incorrect payload size is received.

8.2. Command: Update HMAC Key Register

This command is used by the SPI Flash Controller to update the HMAC-Key register corresponding to the received Counter Address with a new HMAC key calculated based on received input. This command must be issued on every power cycle event on the interface. The HMAC key storage is volatile.



Figure 38. Update HMAC Key Register Sequence Diagram



Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. This command performs two HMAC-SHA-256 operations.

- HMAC-SHA-256 Operation 1 Output = HMAC_Storage[255:0]
 - HMAC Message[31:0] = KeyData[31:0]
 - HMAC Key[255:0] = Root_Key_Register[CounterAddr][255:0]
- HMAC-SHA-256 Operation 2 Output = HMAC-SHA-256 based signature[255:0]
 - HMAC message[63:0] = (OpCode[7:0], CmdType[7:0].CounterAddr[7:0].Reserved[7:0], KeyData[31:0])
 - HMAC Key[255:0] = HMAC_Storage[255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts “successful completion” extended status.

If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

Table 12. Expected Extended Status [7:0] results

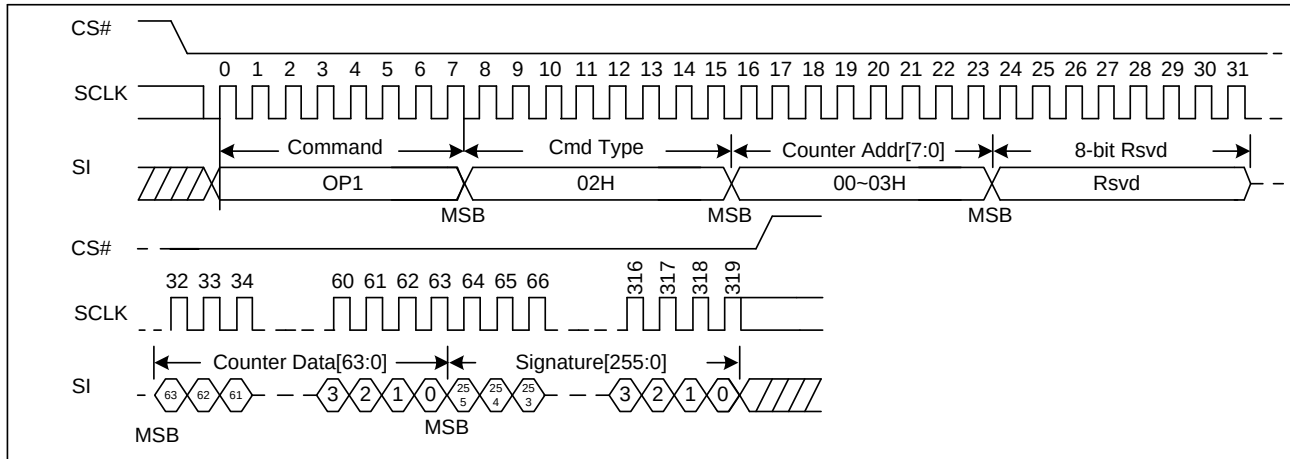
Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	01	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	01	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxx1x	01	This bit is set only when the correct payload size is received. This bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	01	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or incorrect payload size is received.



8.3. Command: Increment Monotonic Counter

This command is used by the SPI Flash Controller to increment the Monotonic counter by 1 inside the SPI Flash Device.

Figure 39. Increment Monotonic Counter Sequence Diagram



The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. The received Counter Data matches the current value of the counter read from the SPI Flash.

- HMAC Message[63:0] = (OpCode[7:0], CmdType[7:0], CounterAddr[7:0], Reserved[7:0], CounterData[31:0])
- HMAC Key[255:0] = HMAC_Key_Register [Counter_Address][255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts “successful completion” extended status. If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

Table 13. Expected Extended Status [7:0] results

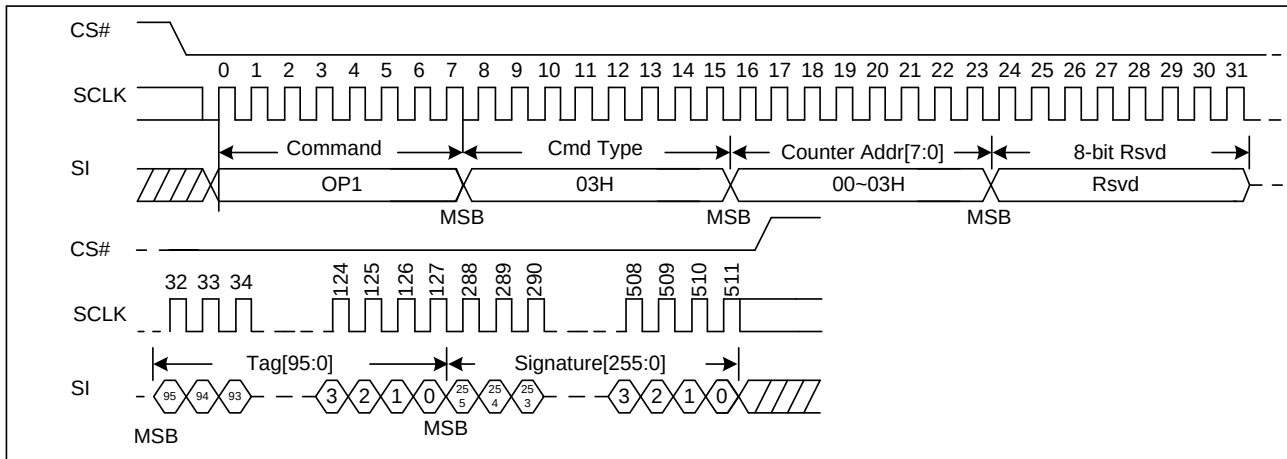
Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	02	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	02	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxx1xx	02	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or incorrect payload size is received.
0xxx1xxx	02	This bit is set only when the correct payload size is received. This bit must be set on HMAC Key Register or Monotonic Counter is uninitialized on previous OP1 command.
0xx1xxxx	02	This bit is set only when the correct payload size is received. The bit must be set when the received counter data filed does not match the actual counter value read from the SPI Flash device.



8.4. Command: Request Monotonic Counter

This command is used by the SPI Flash Controller to request the Monotonic counter value inside the SPI Flash Device.

Figure 40. Request Monotonic Counter Sequence Diagram



The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.

- HMAC Message[127:0] = (OpCode[7:0], CmdType[7:0], CounterAddr[7:0], Reserved[7:0], Tag[95:0])
- HMAC Key[255:0] = HMAC_Key_Register[Counter_Address][255:0]

If the received transaction is error free SPI Flash device successfully executes the command and posts “successful completion” extended status. If the received transaction has errors the SPI Flash does not execute the transaction and posts the corresponding error in extended status.

Table 14. Expected Extended Status [7:0] results

Extended Status[7:0]	Applicable CmdType(s)	Description
10000000	03	This status is set on successful completion (no errors) of OP1 command.
0xxxxx1	03	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxx1xx	03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	03	This bit is set only when the correct payload size is received. This bit must be set on HMAC Key Register or Monotonic Counter is uninitialized on previous OP1 command.

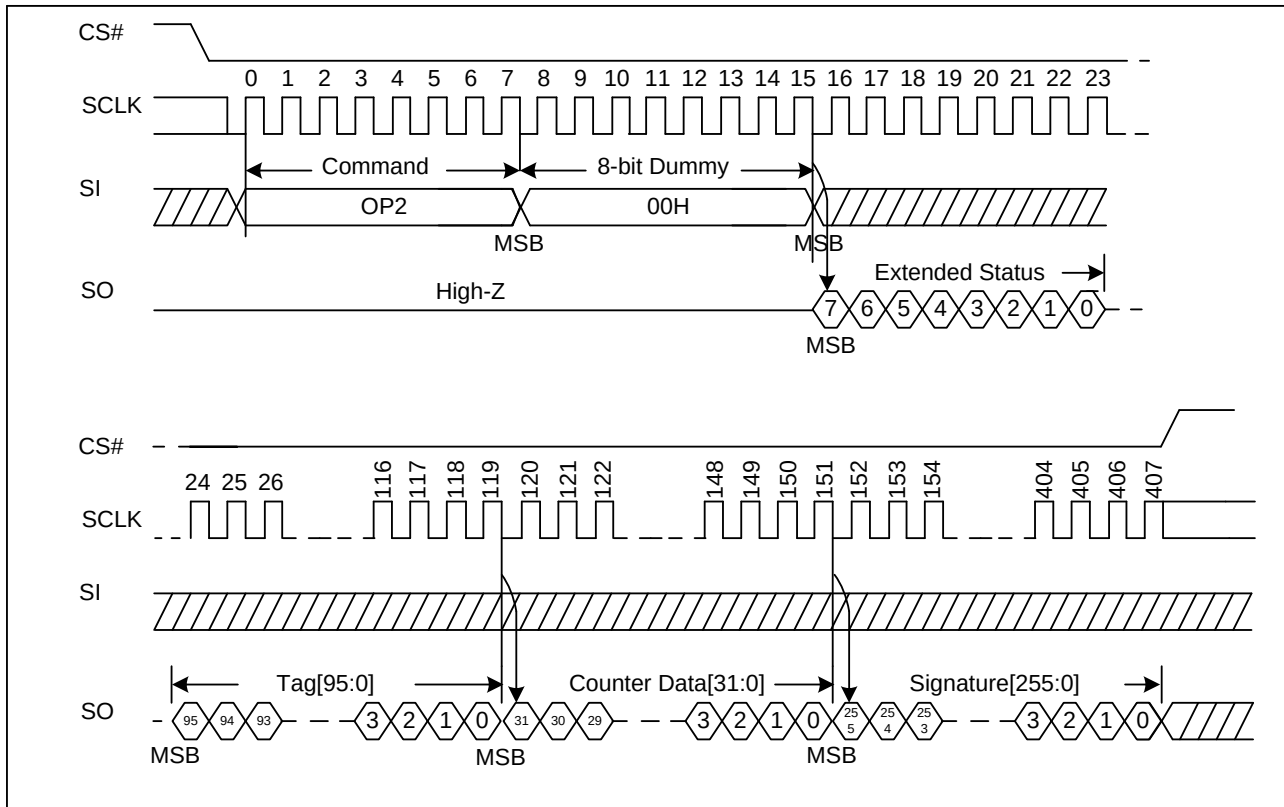
8.5. Command: Read Data

This command is used by the SPI Flash Controller to read extended status from any previously issued OP1 command.



In addition if previous OP1 command is Request Monotonic Counter and if SPI Flash returns successful completion extended status then it returns valid values in the Tag, Counter Data and Signature field. Otherwise the values returned in Tag, Counter and Signature field are invalid. The controller may abort the read prematurely prior to completely reading the entire payload. This may occur when the controller wants to simply read the extended status or when it observes an error being returned in the extended status field. The controller may also continue reading past the defined payload size of 49 bytes. Since this is an error condition, the SPI Flash may return any data past the defined payload size. The controller must ignore the data.

Figure 41. Read Data Sequence Diagram



If previous OP1 command is Request Monotonic Counter and if SPI Flash returns successful completion extended status then it returns valid values in the Tag, Counter Data and Signature field. It calculates HMAC-SHA-256 signatures based on following parameters.

- HMAC Message[127:0] = Tag [95:0], Counter_Data_Read[31:0]
- HMAC Key[255:0] = HMAC_Key_Register[Counter_Address][255:0]



Table 15. Extended Status Register Definition

Extended Status[7:0]	Applicable CmdType(s)	Description
00000000	-	Power On State (OP2 issued directly after power-up).
10000000	00, 01, 02, 03	This status is set on successful completion (no errors) of OP1 command.
0xxxxxx1	00, 01, 02, 03,	This bit is set to 1, when device is busy executing OP1 command. It is reset to 0 when OP1 command execution is done.
0xxxxx1x	00, 01	This bit is set only when the correct payload size is received. When cmdtype = 0, this error bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For remaining cmdtype = 1 this bit is set when the corresponding monotonic counter is uninitialized
0xxxx1xx	01, 02, 03	This bit is set on Signature Mismatch, Counter Address out of range when correct payload size is received; or Cmdtype is out of range; or incorrect payload size is received.
0xxx1xxx	02, 03	This bit is set on HMAC Key Register or Monotonic Counter uninitialized on previous OP1 command when correct payload size is received
0xx1xxxx	02	This bit is set on Counter Data Mismatch on previous increment when correct payload size is received
0x1xxxxx	-	Fatal Error. It is set when no valid counter is found after initialization.
Current value	-	Extended status register will not be updated until first 8 bits of OP1 is received. The correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.



8.6. Operations Allowed/Disallowed During RPMC Operation

In the deep power down state OP1, OP2 commands are ignored until the part comes out of deep power down state.

WREN state does not affect the OP1 command execution inside the SPI Flash.

Suspend operation can be used to execute high-priority reads from the flash device while a long-latency operation is underway. However, OP1 is not recommended when the flash device is in WIP or suspended state.

In the table below, OP1 state is defined as the time starting with a transaction with OP1 op-code sent to the device and ending when the device clears the extended status busy bit. During OP1 state if a suspend transaction is received, the SPI Flash will ignore the suspend command and continue with the execution of the current OP1 command as described in the table below. P/E state is defined as the time starting with a transaction with write or erase op-code sent to the device and ending when the device clears the status busy bit. P/E Suspended State starts when the device sets the program suspend status done bit after receiving a program suspend op-code. During P/E State and P/E Suspended State, OP1 is also allowed but not recommended

The table below shows all operation support in each state.

Table 16. RPMC Operation

Operation	OP1 state	P/E state	P/E Suspended State
Suspend	Ignored	Yes-> P/E Suspended State(not chip erase or write status operation) No ->remain P/E state (chip erase or write status operation)	No
Resume	Ignored	No	Yes -> P/E state
All reads except Read status	Yes	No	Yes
All writes/erases	Yes	No	No
OP1	No	Yes but not recommended	Yes but not recommended
Write status	Yes	No	No
OP2	Yes->OP1 busy state (when extended status busy is 1) ->OP1 done state (when extended status busy is 0)	Yes. Will indicate the status associated with the OP1 operation.	Yes. Will indicate the status associated with the OP1 operation
Read status	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.	Yes. Will indicate the busy state associated with the subsequent transaction issued to the SPI Flash.



9. ELECTRICAL CHARACTERISTICS

9.1. POWER-ON TIMING

Figure 73 Power-On Timing Sequence Diagram

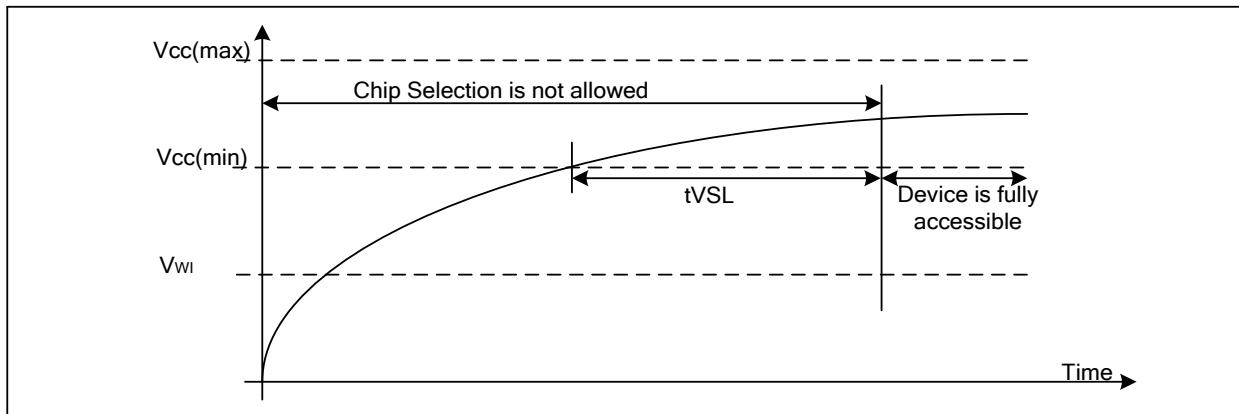


Table 21 Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC (min) To CS# Low	2.5		ms
VWI	Write Inhibit Voltage	1.5	2.5	V

9.2. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register bits are set to 0, except QE bit (S9) and DRV0 bit (S21) are set to 1.

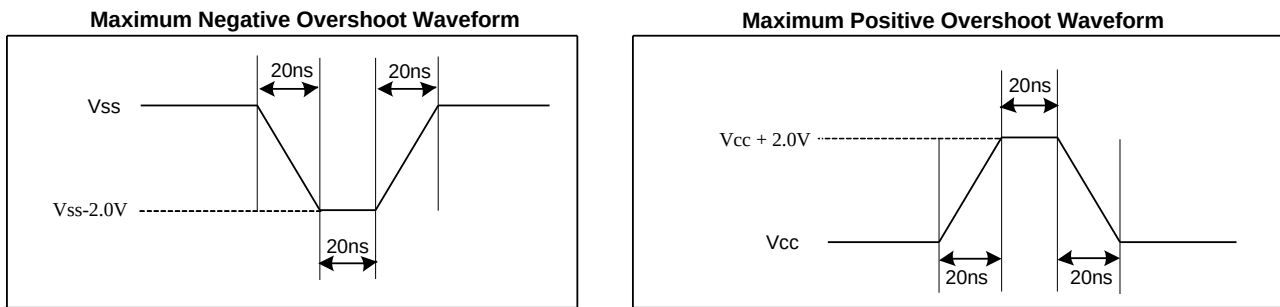
9.3. ABSOLUTE MAXIMUM RATINGS

Table 22 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V



Figure 74 Input Test Waveform and Measurement Level

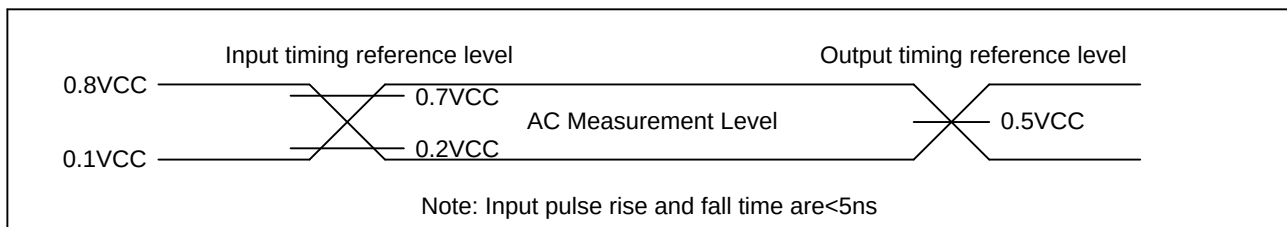


9.4. CAPACITANCE MEASUREMENT CONDITIONS

Table 23 Capacitance Measurement Conditions

Symbol	Parameter	Min	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			12	pF	VIN=0V
COUT	Output Capacitance			16	pF	VOUT=0V
CL	Load Capacitance	30			pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 75 Input/Output Timing Reference Level





9.5. DC CHARACTERISTICS

Table 24 DC CHARACTERISTICS (T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I _{LI}	Input Leakage Current				±4	μA
I _{LO}	Output Leakage Current				±4	μA
I _{CC1}	Standby Current	CS#=VCC, V _{IN} =VCC or VSS		13	55	μA
I _{CC2}	Deep Power-Down Current	CS#=VCC, V _{IN} =VCC or VSS		2	13	μA
I _{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)		15	25	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	20	mA
I _{CC4}	Operating Current (PP)	CS#=VCC			25	mA
I _{CC5}	Operating Current (WRSR)	CS#=VCC			25	mA
I _{CC6}	Operating Current (SE)	CS#=VCC			25	mA
I _{CC7}	Operating Current (BE)	CS#=VCC			25	mA
I _{CC8}	Operating Current (CE)	CS#=VCC			25	mA
V _{IL}	Input Low Voltage		-0.5		0.2VCC	V
V _{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V _{OL}	Output Low Voltage	I _{OL} =100μA			0.2	V
V _{OH}	Output High Voltage	I _{OH} =-100μA	VCC-0.2			V

Note:

1. Typical value at T = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.



9.6. AC CHARACTERISTICS

Table 25 AC CHARACTERISTICS (T= -40°C~85°C, VCC=2.7~3.6V, CL=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f _{C1}	Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output (3BH, 3CH), Quad Output (6BH, 6CH), Fast Read (0BH, 0CH) instructions, on 3.0 – 3.6V power supply			104	MHz
f _{C2}	Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output (3BH, 3CH), Quad Output (6BH, 6CH), Fast Read (0BH, 0CH) instructions, on 2.7 – 3.0V power supply			80	MHz
f _R	Serial Clock Frequency For: Read (03H, 13H)			50	MHz
t _{CLH}	Serial Clock High Time	3.7			ns
t _{CLL}	Serial Clock Low Time	3.7			ns
t _{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t _{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t _{SLCH}	CS# Active Setup Time	8			ns
t _{CHSH}	CS# Active Hold Time	5			ns
t _{SHCH}	CS# Not Active Setup Time	5			ns
t _{CHSL}	CS# Not Active Hold Time	5			ns
t _{SHSL}	CS# High Time (Read/Write)	20			ns
t _{SHQZ}	Output Disable Time			6	ns
t _{CLQX}	Output Hold Time	1.8			ns
t _{DVCH}	Data In Setup Time	2			ns
t _{CHDX}	Data In Hold Time	2			ns
t _{CLQV}	Clock Low To Output Valid			7	ns
t _{DP}	CS# High To Deep Power-Down Mode			20	μs
t _{RES1}	CS# High To Standby Mode Without Electronic Signature Read			30	μs
t _{RES2}	CS# High To Standby Mode With Electronic Signature Read			30	μs
t _{SUS}	CS# High To Next Command After Suspend			20	μs
t _{RS}	Latency Between Resume And Next Suspend	100			μs
t _{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t _{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t _W	Write Status Register Cycle Time		5	20	ms
t _{BP1}	Byte Program Time (First Byte)		30	50	μs
t _{BP2}	Additional Byte Program Time (After First Byte)		2.5	12	μs
t _{PP}	Page Programming Time		0.4	2.4	ms
t _{SE}	Sector Erase Time		70	400	ms
t _{BE1}	Block Erase Time (32K Bytes)		0.16	0.8	s
t _{BE2}	Block Erase Time (64K Bytes)		0.22	1	s



3.3V Uniform Sector GigaDevice Dual and Quad Serial Flash

GD25R256D

t_{CE}	Chip Erase Time (GD25R256D)		70	200	s
t_{WRKR}	Write Root key register		3	5.5	ms
t_{UHKR}	Update HMAC Key Register		120		us
t_{IMC}	Increment Monotonic Counter		20	300	ms
t_{RMC}	Request Monotonic Counter		100	1200	us

Note:

1. Typical value tested at $T = 25^{\circ}\text{C}$.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 76 Serial Input Timing

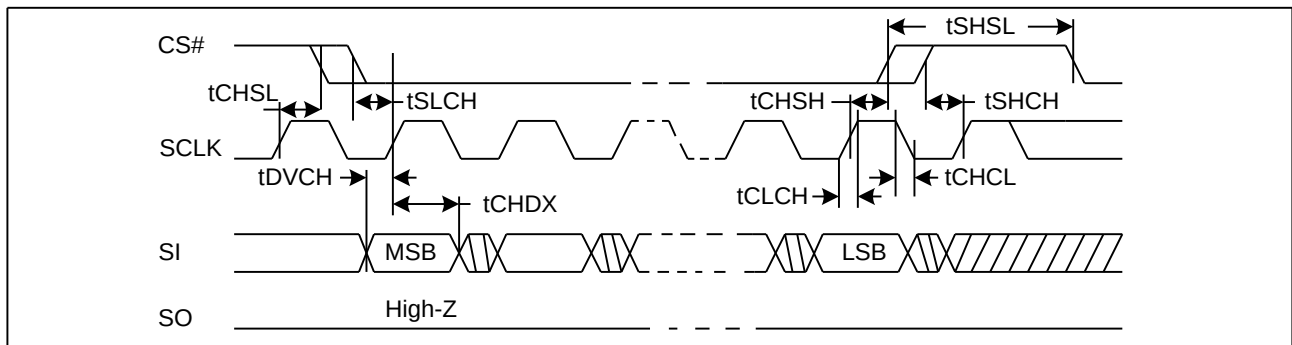


Figure 77 Output Timing

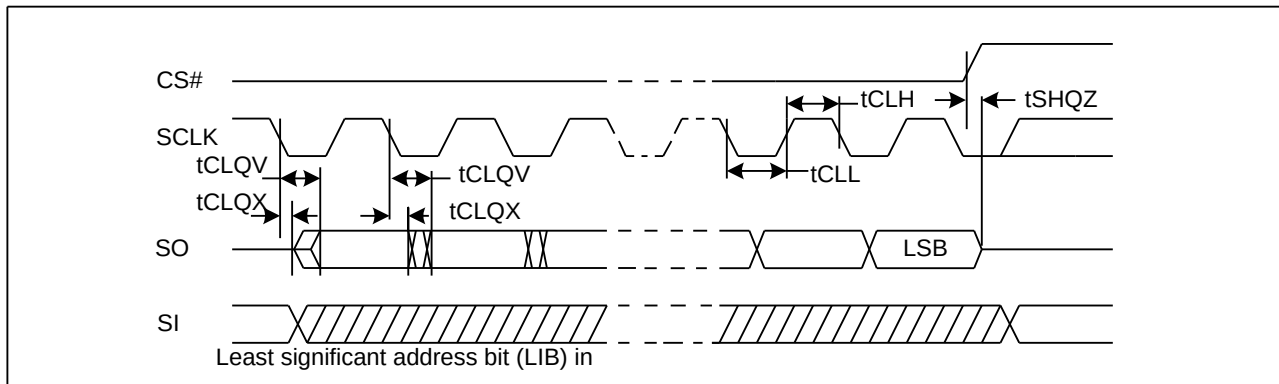
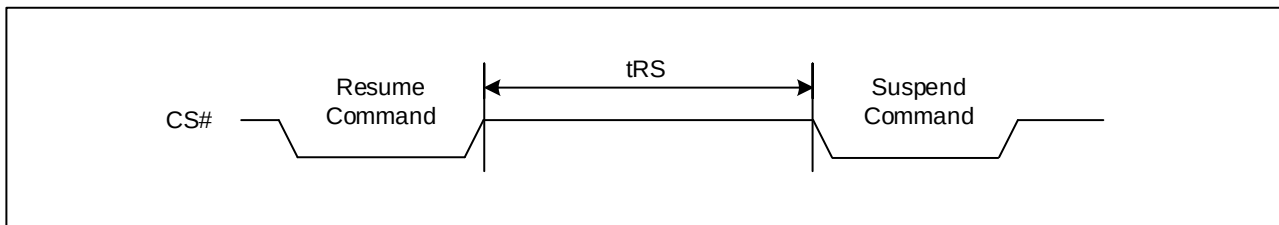


Figure 78. Resume to Suspend Timing Diagram





10. ORDERING INFORMATION

GD	XX	XX	XX	X	X	X	X	X	
									Packing T or no mark: Tube Y: Tray R: Tape and Reel
									Green Code G: Pb Free + Halogen Free Green Package R: Pb Free + Halogen Free Green Package + RESET# Pin
									Temperature Range I: Industrial (-40°C to +85°C)
									Package Type F: SOP16 300mil Y: WSON8 (8x6mm) B: TFBGA-24ball (5x5 Ball Array)
									Generation D: D Version
									Density 256: 256M bit
									Series R: 3V, 4KB Uniform Sector, RPMC
									Product Family 25: SPI NOR Flash



10.1. Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

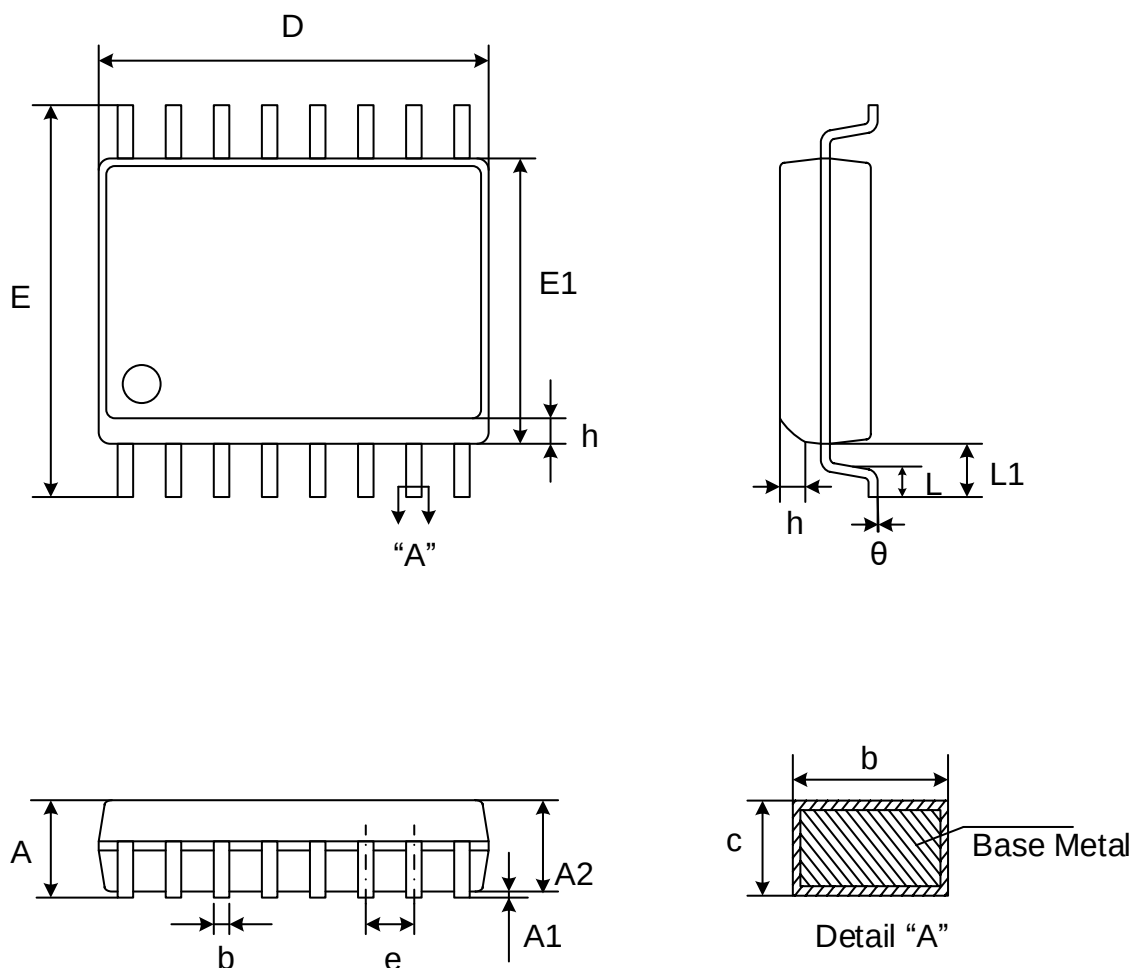
Temperature Range I: Industrial (-40°C to +85°C)

Product Number	Density	Package Type
GD25R256DFIG	256Mbit	SOP16 300mil
GD25R256DFIR		
GD25R256DYIG	256Mbit	WSO8 (8x6mm)
GD25R256DBIG	256Mbit	TFBGA-24ball (5x5 Ball Array)
GD25R256DBIR		



11. PACKAGE INFORMATION

11.1. Package SOP16 300MIL



Dimensions

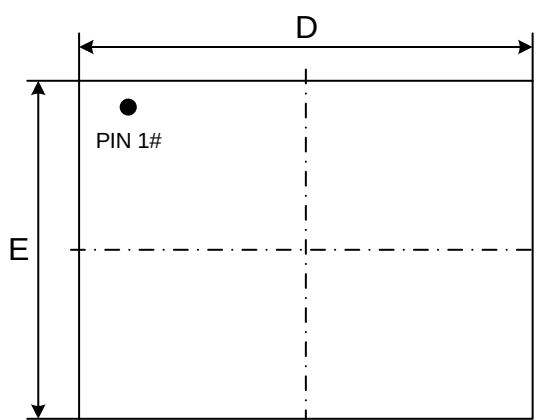
Symbol		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
Unit														
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	-
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8

Note:

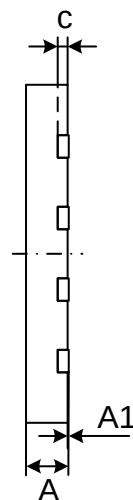
1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.



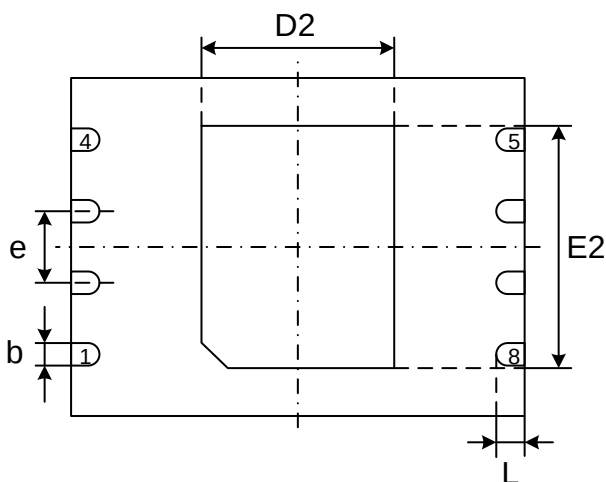
11.2. Package WSON8 (8*6mm)



Top View



Side View



Bottom View

Dimensions

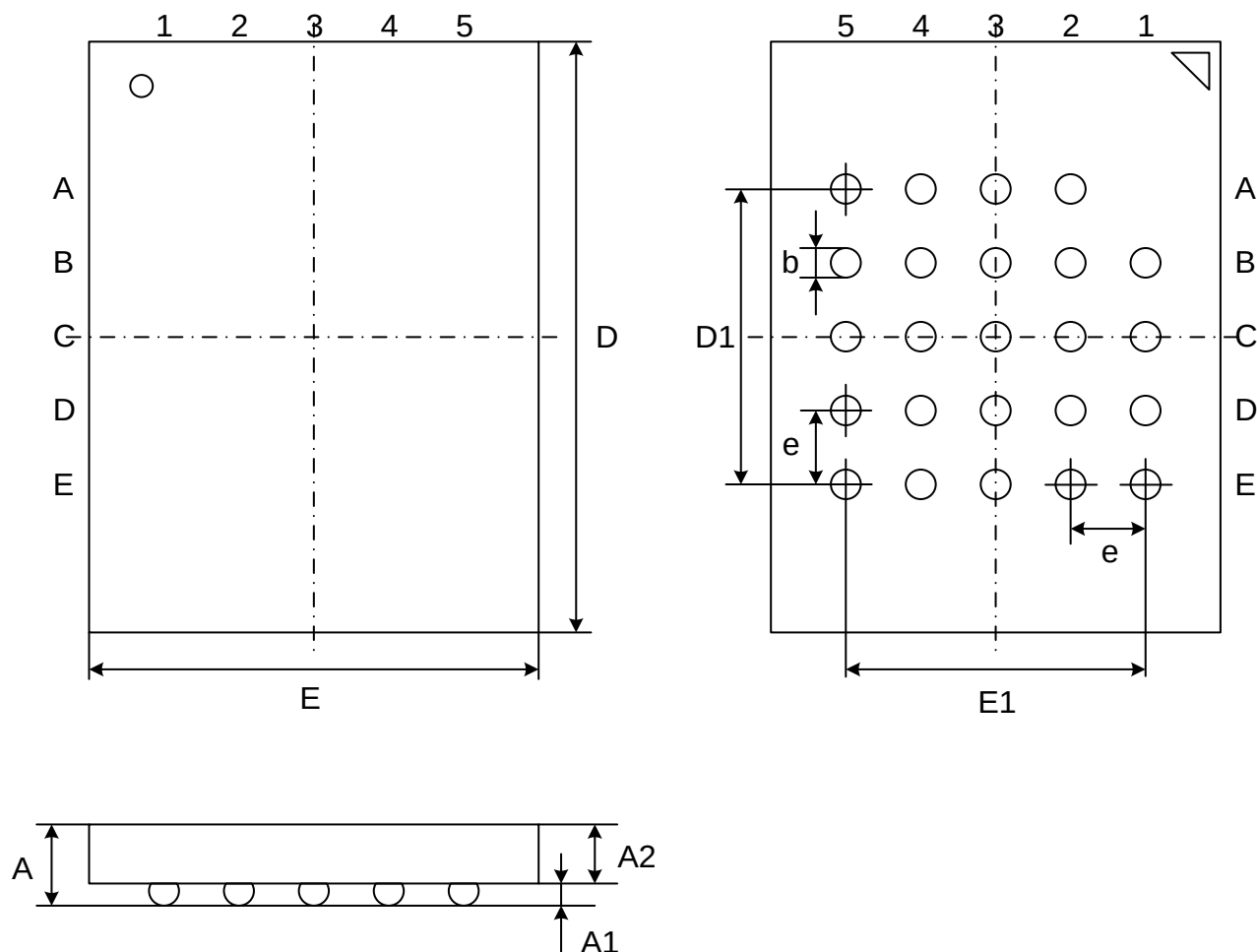
Symbol		A	A1	c	b	D	D2	E	E2	e	L
Unit											
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55

Note:

- Both the package length and width do not include the mold flash.
- The exposed metal pad area on the bottom of the package is floating.
- Coplanarity $\leq 0.08\text{mm}$. Package edge tolerance $\leq 0.10\text{mm}$.
- The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.



11.3. Package TFBGA-24BALL (5*5 ball array)



Dimensions

Symbol		A	A1	A2	b	E	E1	D	D1	e
Unit										
mm	Min		0.25	0.75	0.35	5.90	4.00	7.90	4.00	1.00
	Nom		0.30	0.80	0.40	6.00		8.00		
	Max	1.20	0.35	0.85	0.45	6.10		8.10		

Note: Both the package length and width do not include the mold flash.



12. REVISION HISTORY

Version No.	Description	Page	Date
1.0	Initial Release	All	2017-12-5
1.1	Modify the sequence diagram of 42H command Modify tVSL min value from 5ms to 2.5ms Modify CIN max value from 6pF to 12pF Modify COUT max value from 8pF to 16pF Modify ILI and ILO from $\pm 2\mu\text{A}$ to $\pm 4\mu\text{A}$ Modify Icc1 from 15-50 μA to 13-55 μA Modify Icc2 from 1-8 μA to 2-13 μA Add tRS, of which the min value is 100 μs Modify tw typ. value from 1ms to 5ms Modify tpp typ.value from 0.6ms to 0.4ms Modify tBE1 typ.value from 0.2s to 0.16s Modify tBE2 typ.value from 0.3s to 0.22s Modify tCE form 100~240s to 70~200s	P58 P71 P72 P72 P73 P73 P73 P74 P74 P74 P74 P75 P75	2019-2-19
1.2	Modify the description of DRV bits	P14	2019-4-17
1.3	Add RMPC Commands Description Add t _{WRKR} , t _{UHKR} , t _{IMC} , t _{PMC} Update Ordering Information	P61-69 P74 P75, 76	2020-3-3



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